

Fig 1

Transmit 201

Receive 202

TX:ctrl RX:ctrl

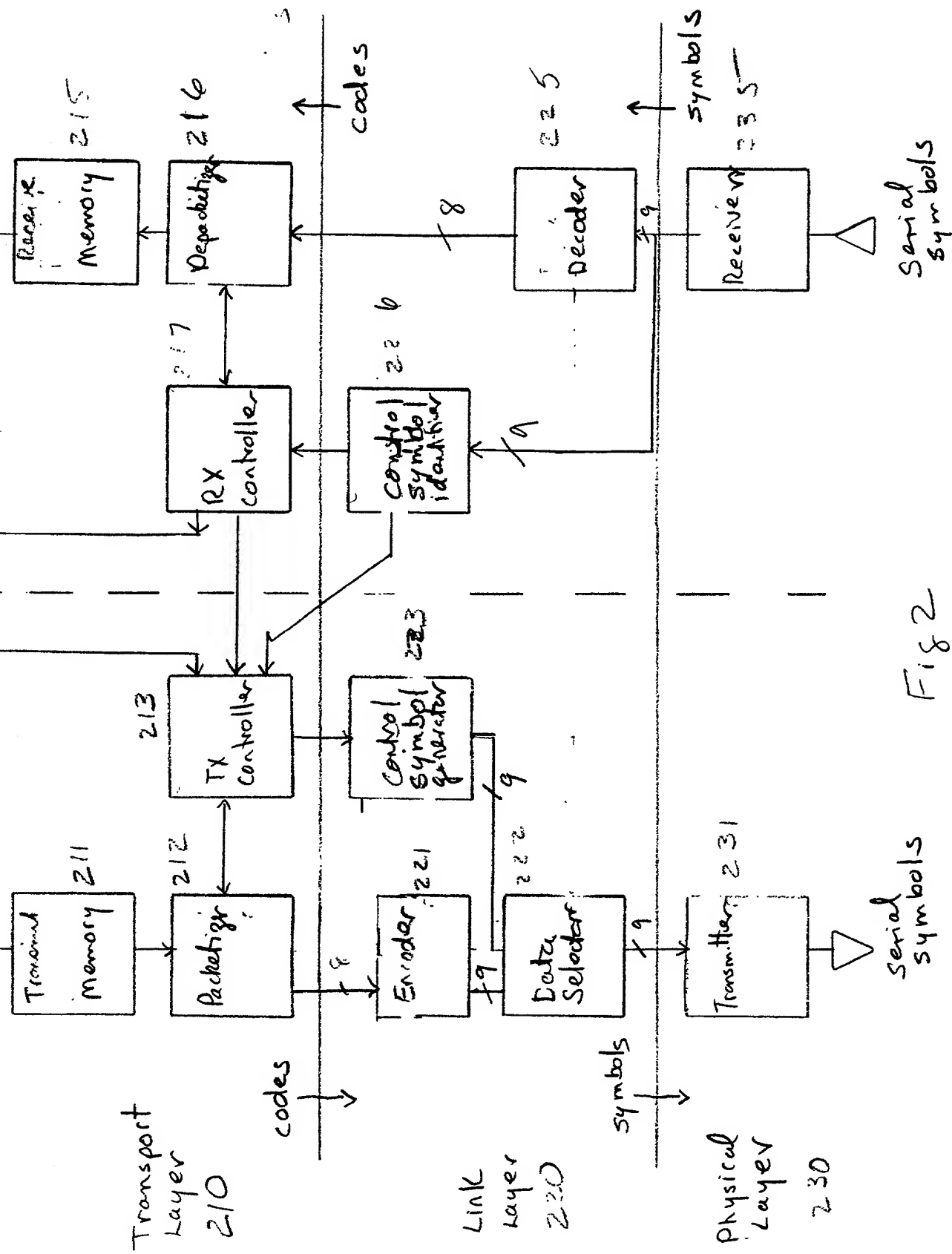


Fig 2

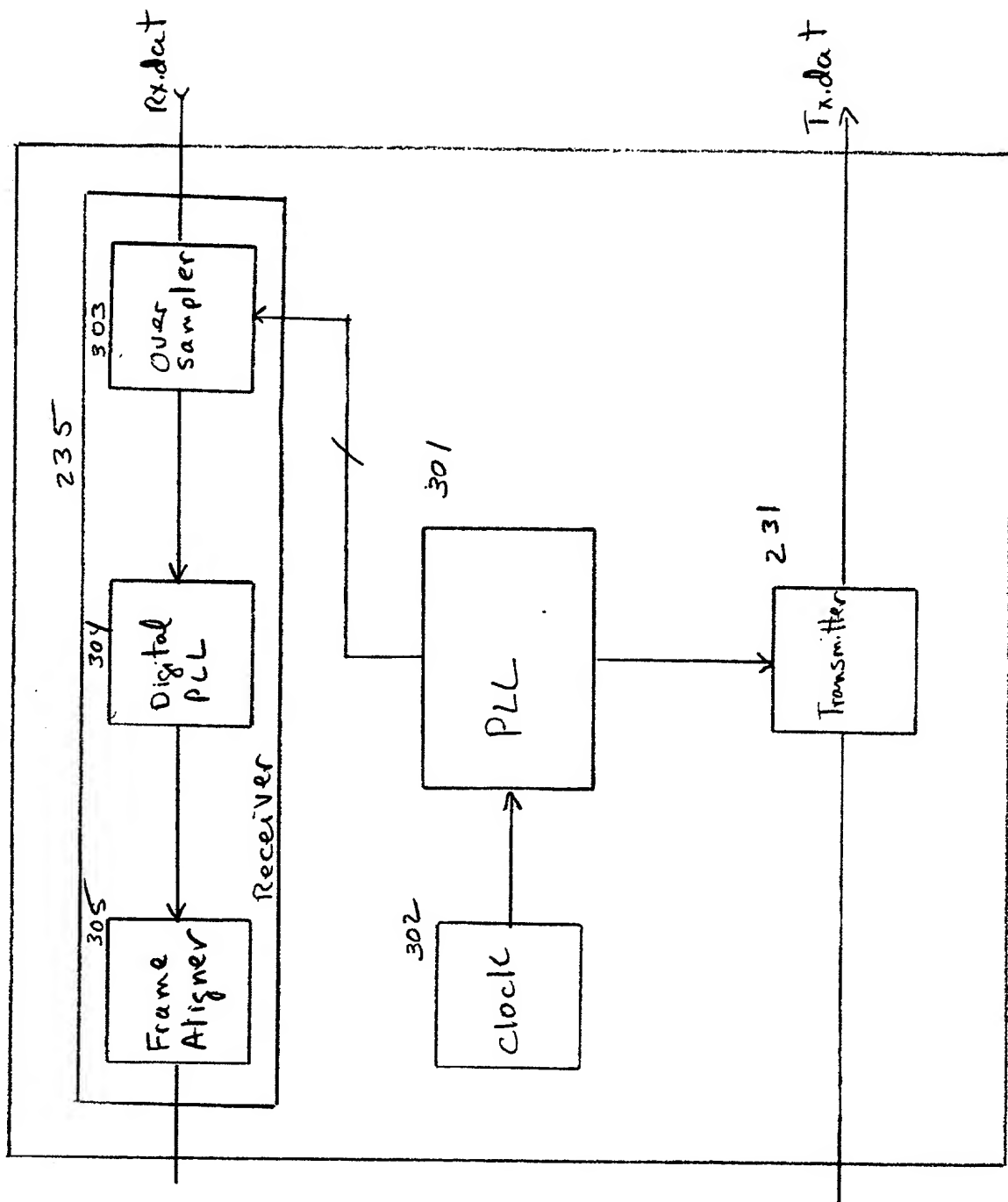


Fig 3

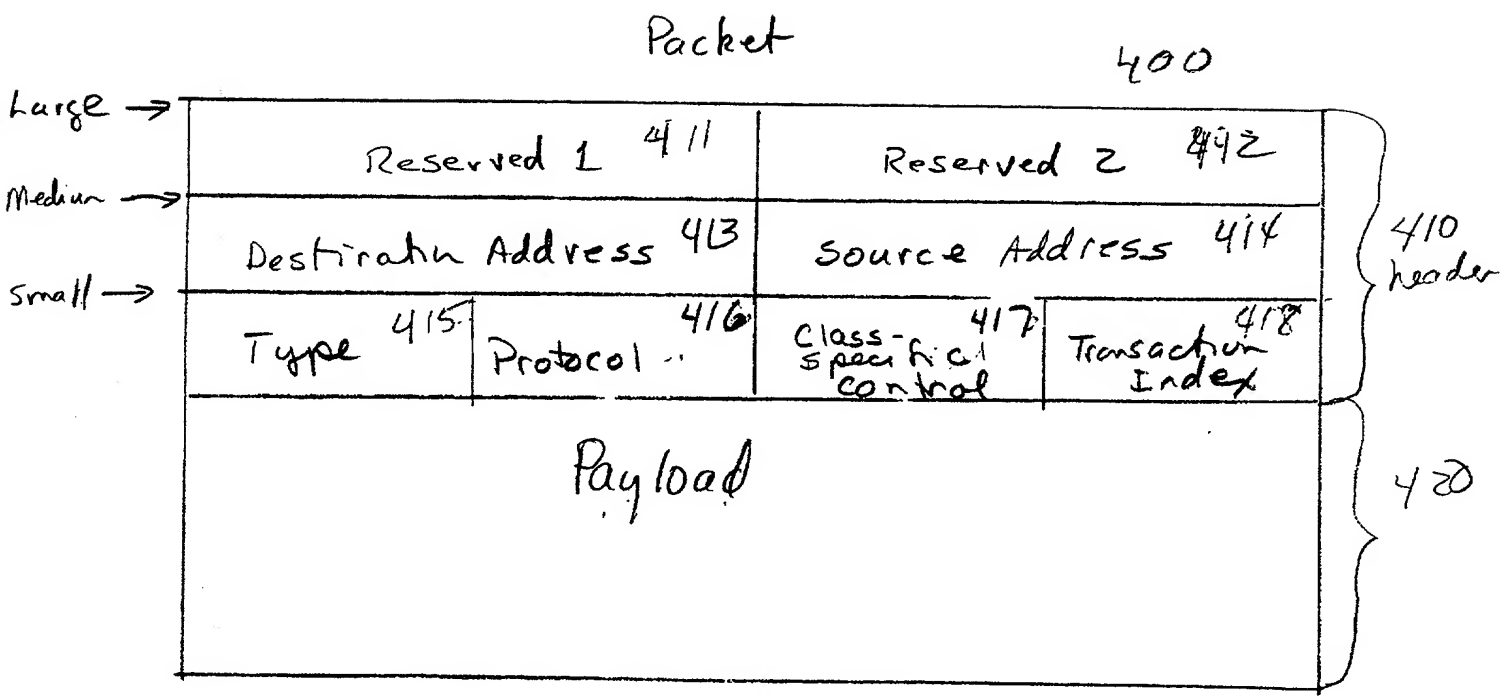
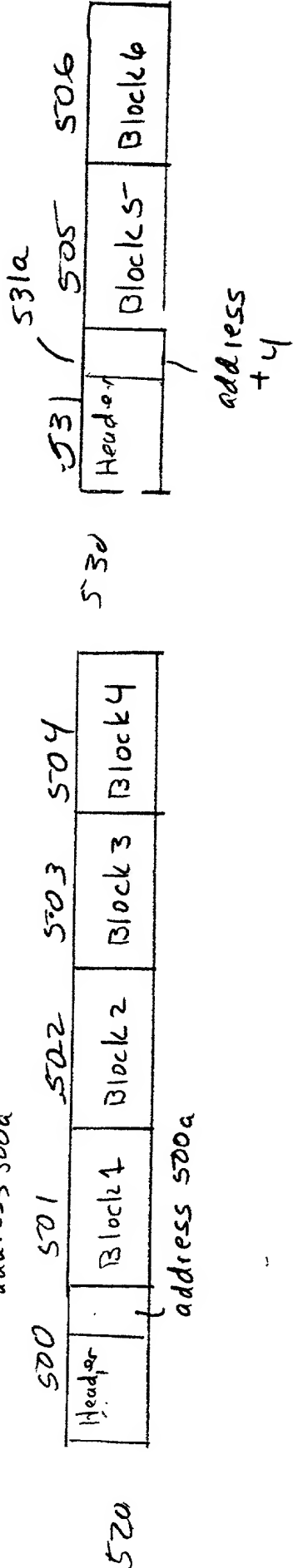
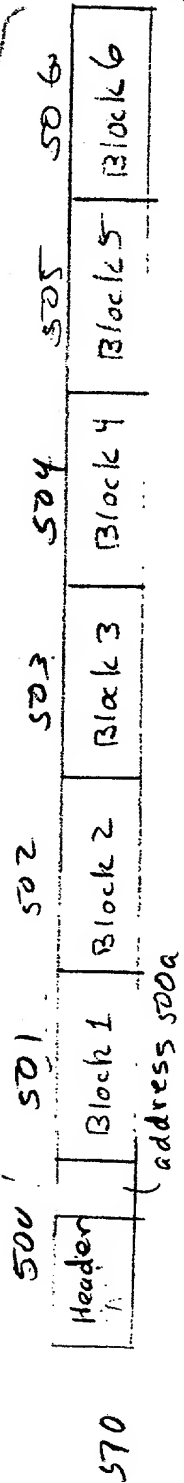


Fig 4

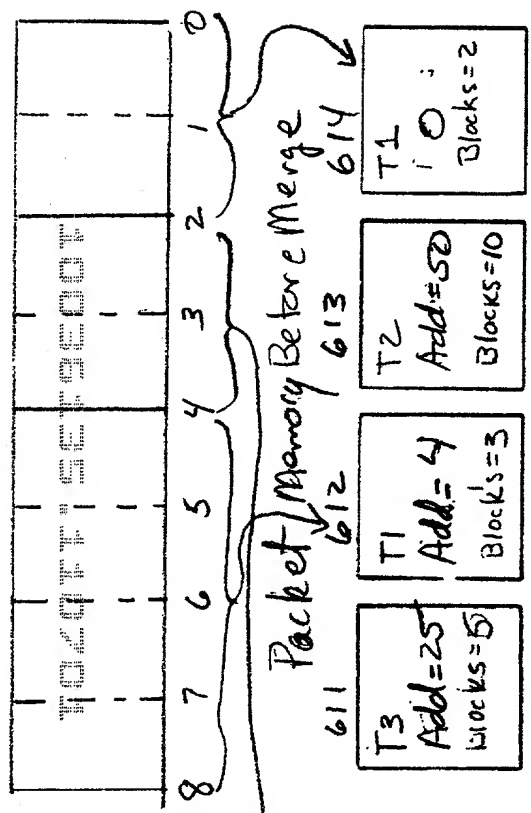
payload 511

FOOTER



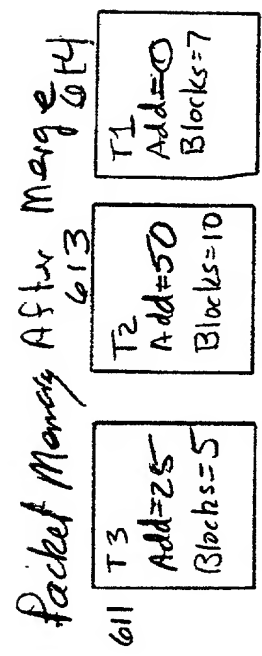
F. 35

600 T:1



Received Packet  
T1  
Add = 2  
Blocks = 2

630



F. 86

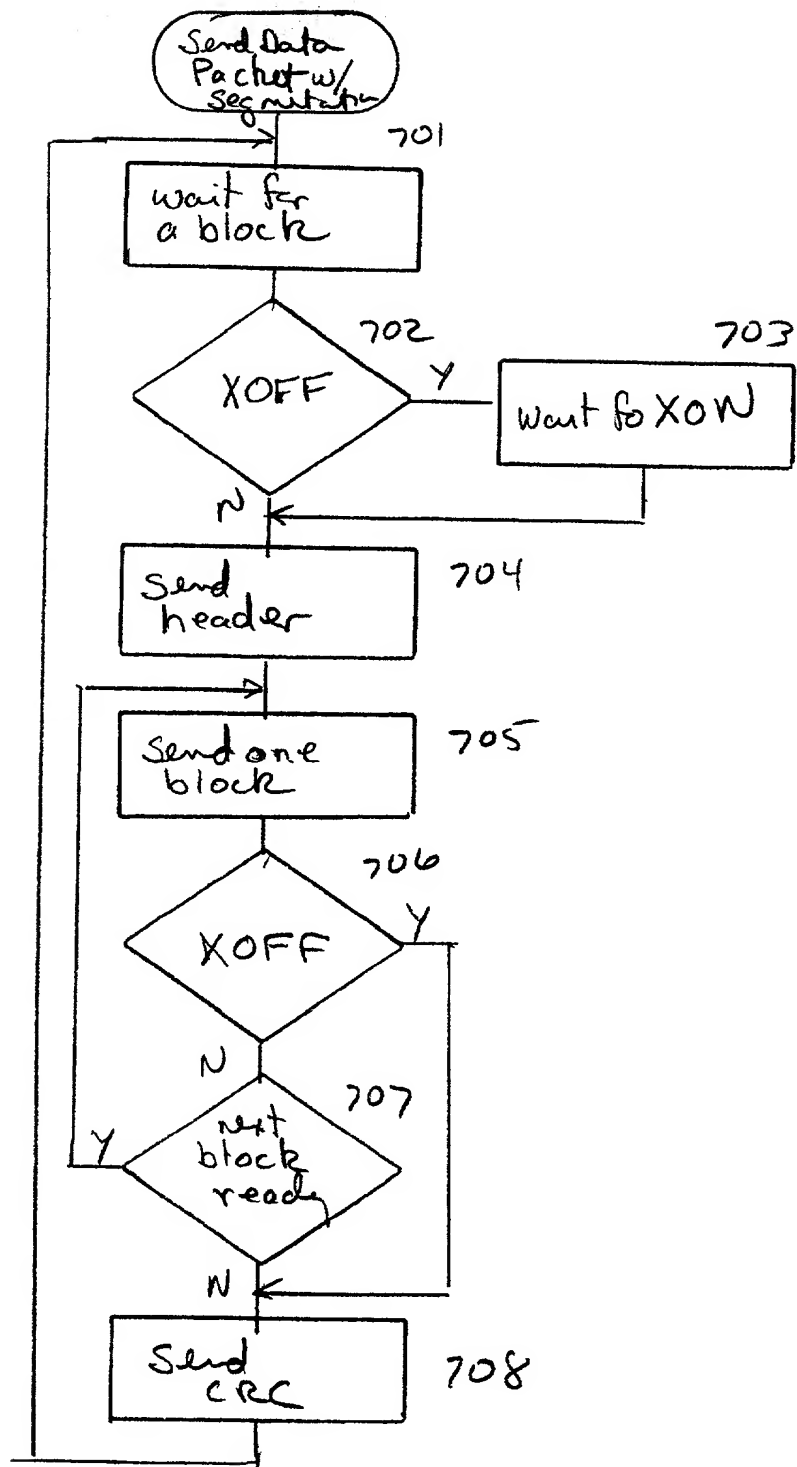


Fig 7

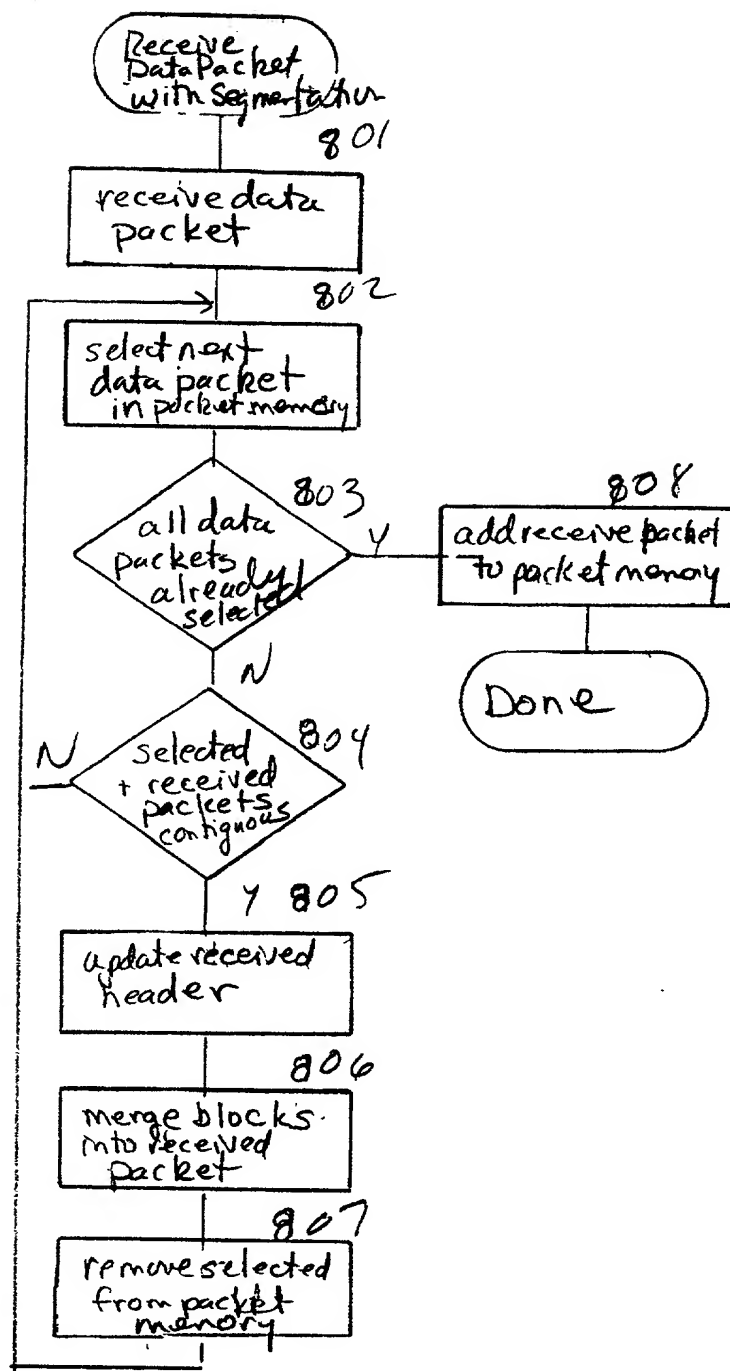
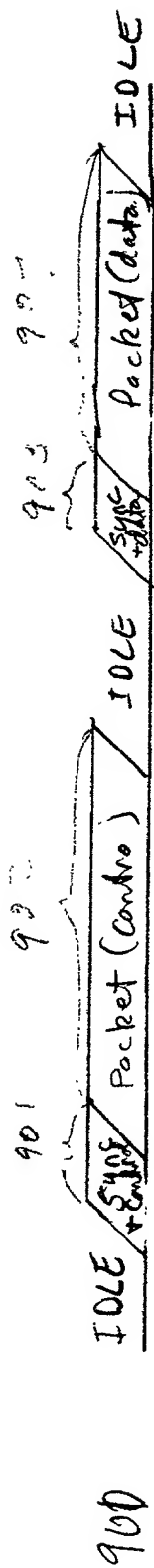


Fig 8





Sync + packet type

Fig 9A

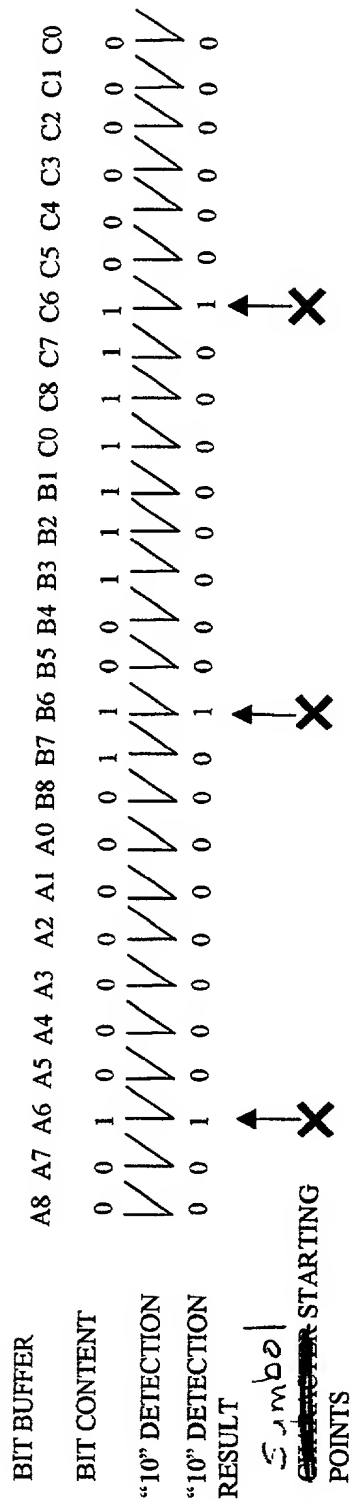


Fig 9B

910

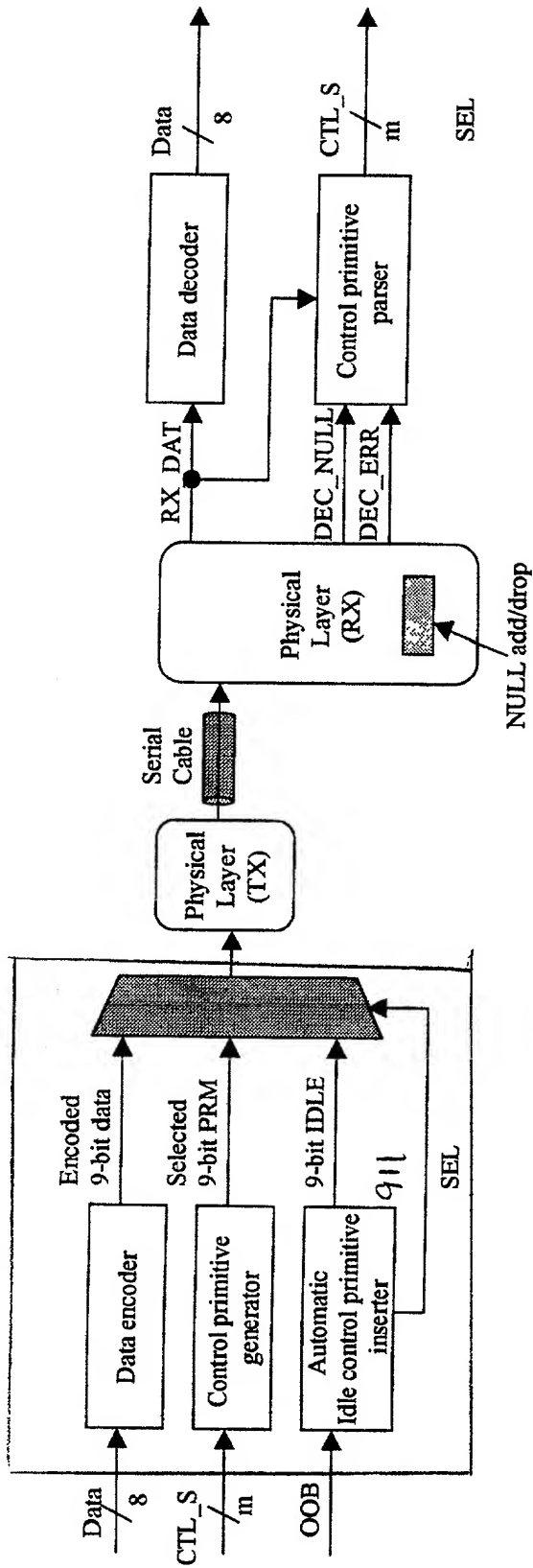


Fig. 9C

~~TOP SECRET~~

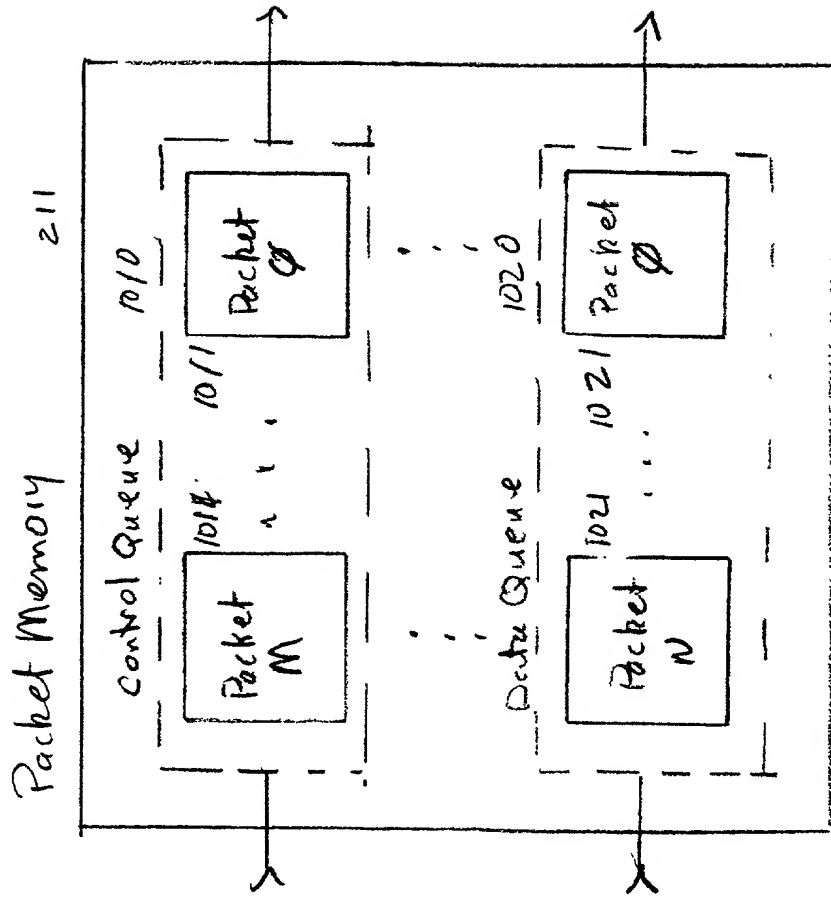


Fig 10

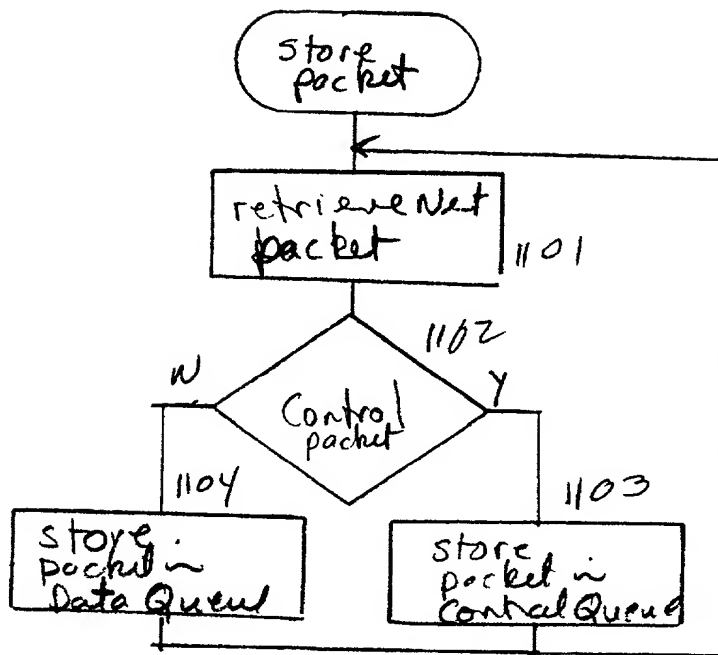


Fig 11

4036435 40704

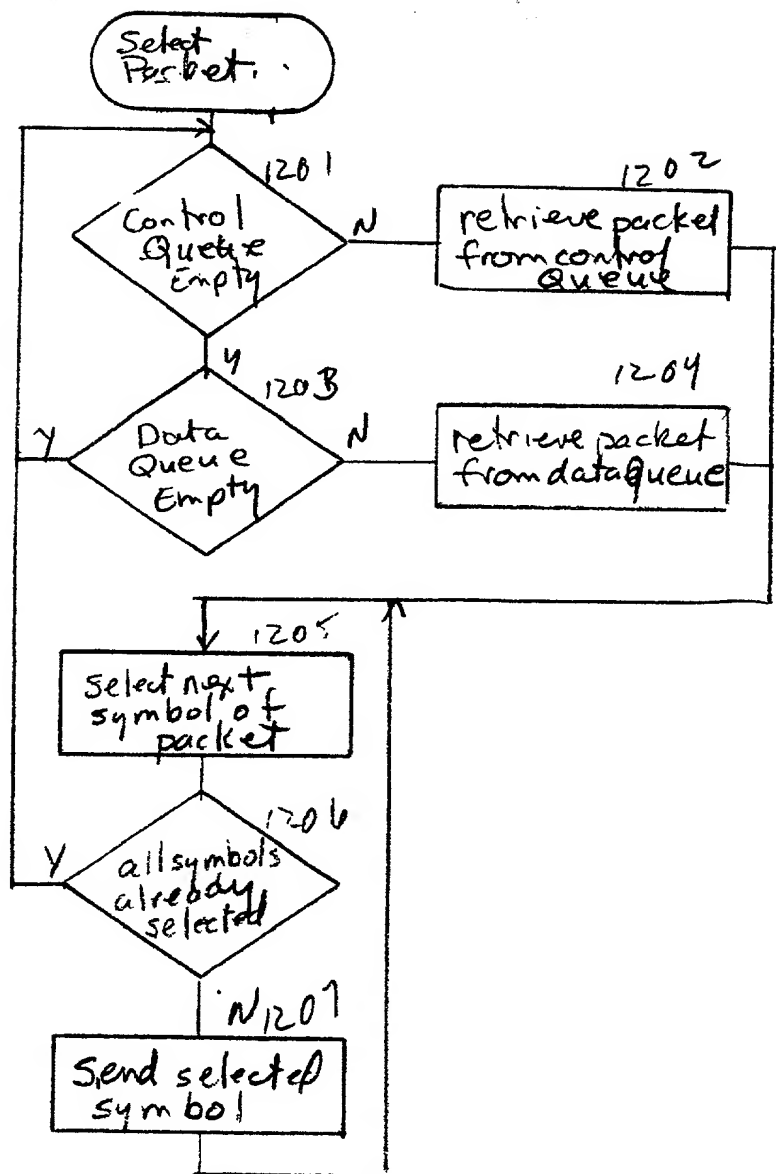


Fig 12

4036435 40364

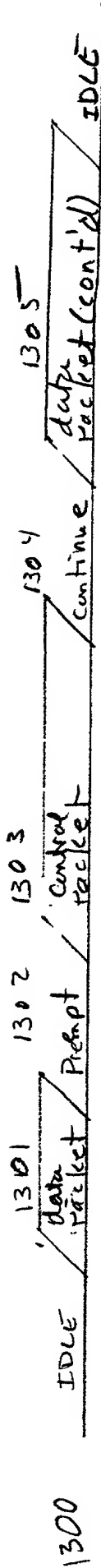


Fig 13

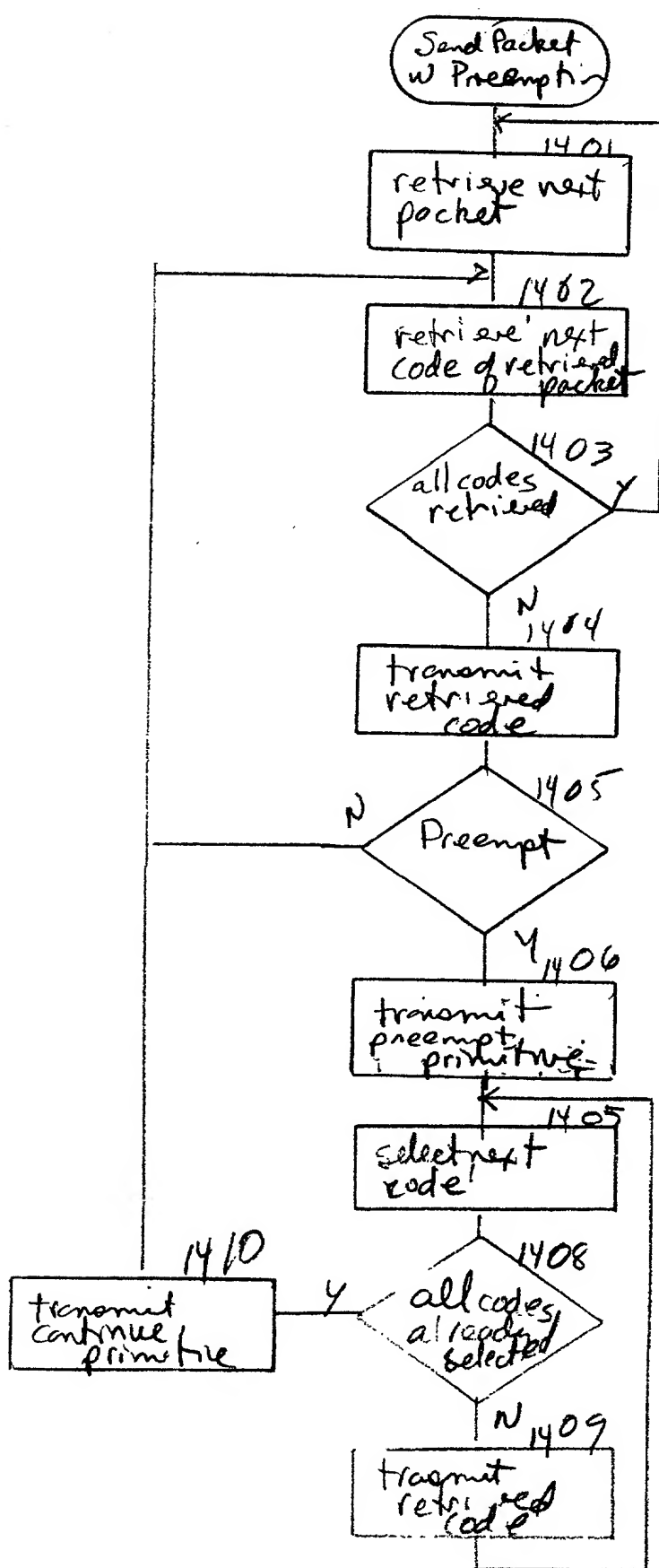


Fig 14



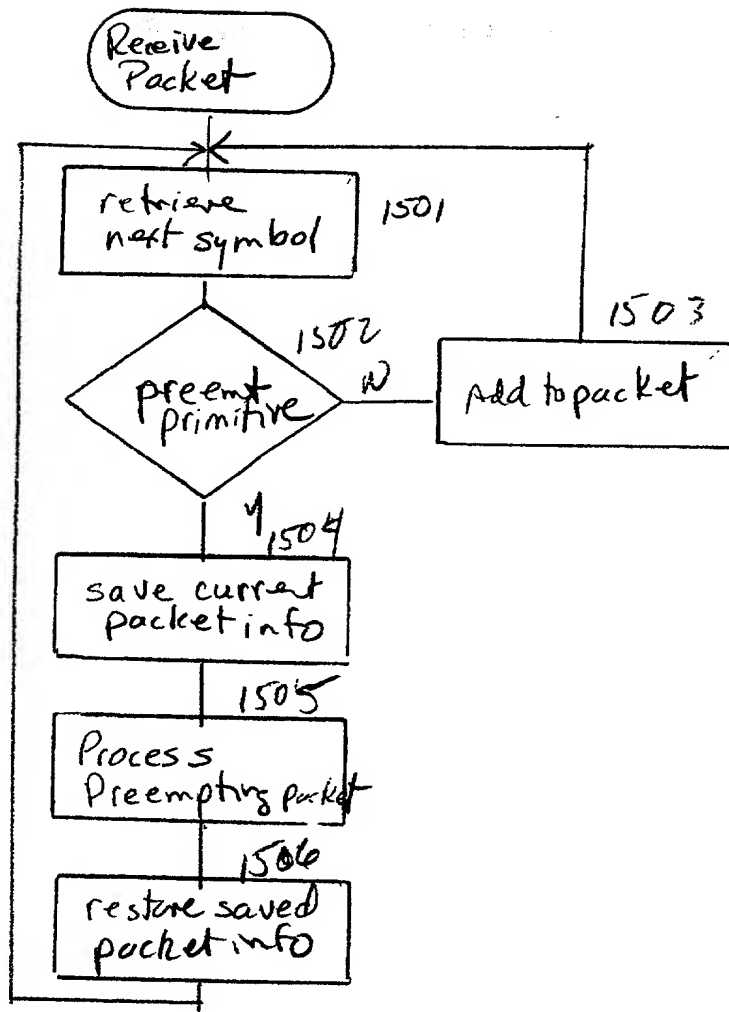


Fig 15

# Switch Network

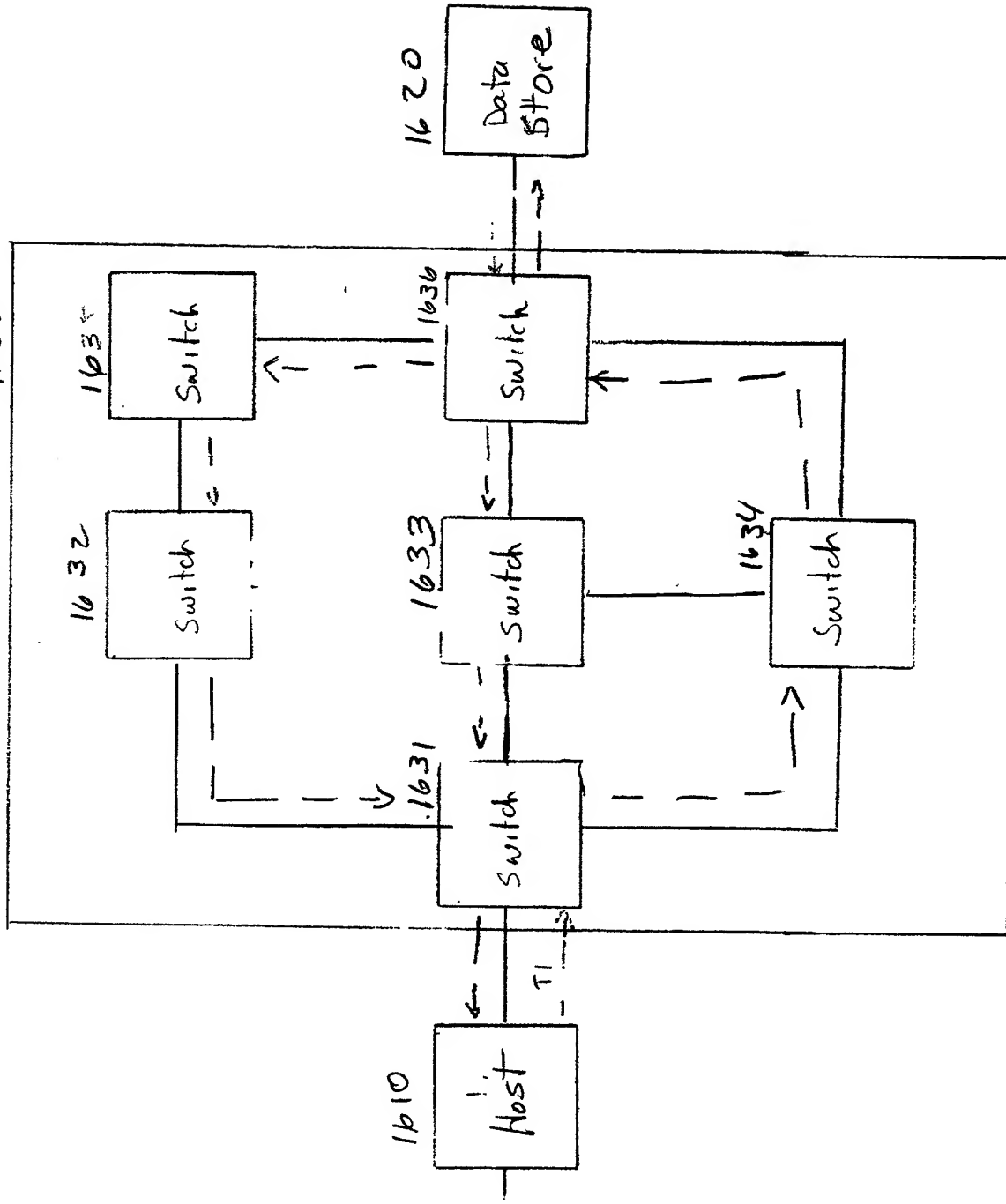
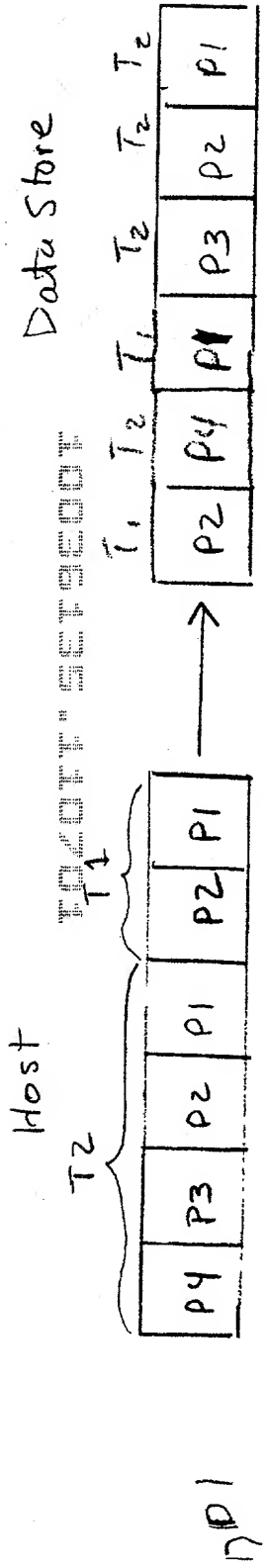
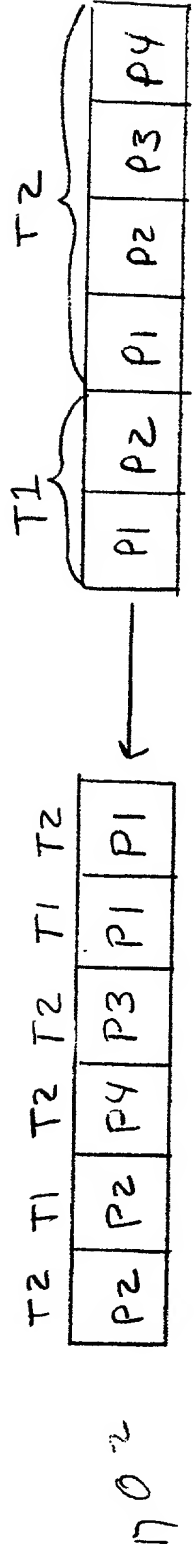


Fig 16



Preserving Packet Order w/ Transaction



No Packet or Transaction Ordering

Fig 17

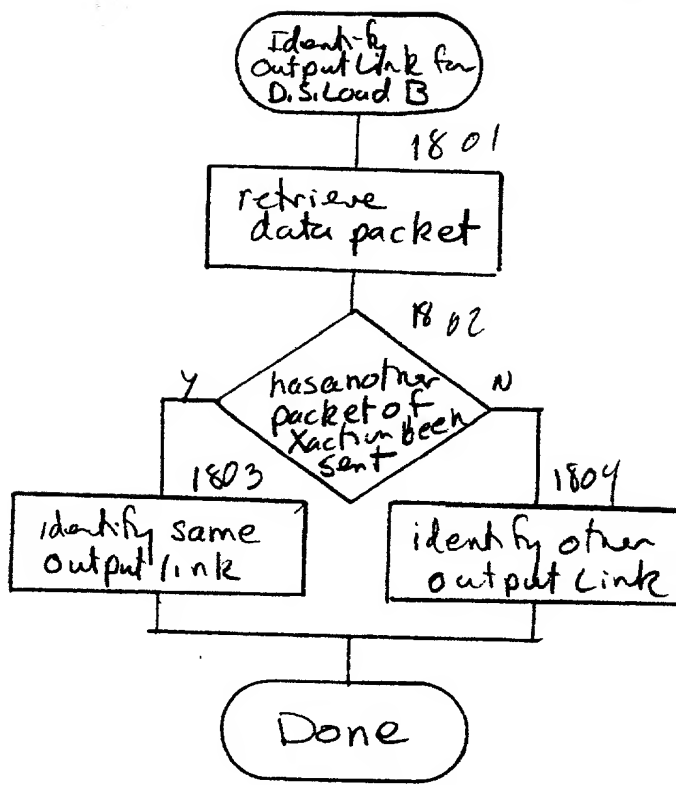


Fig 18

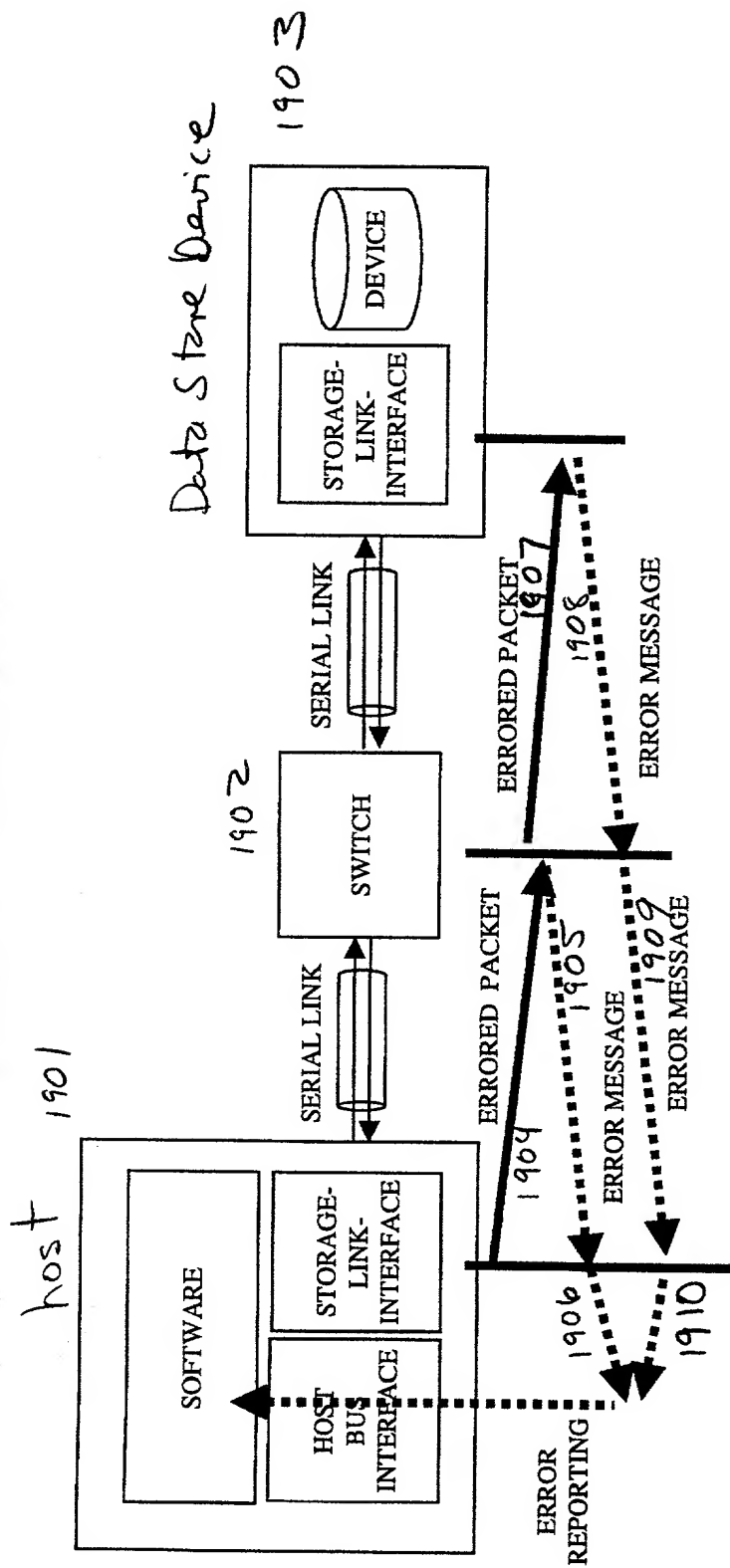


Fig 19A

1901

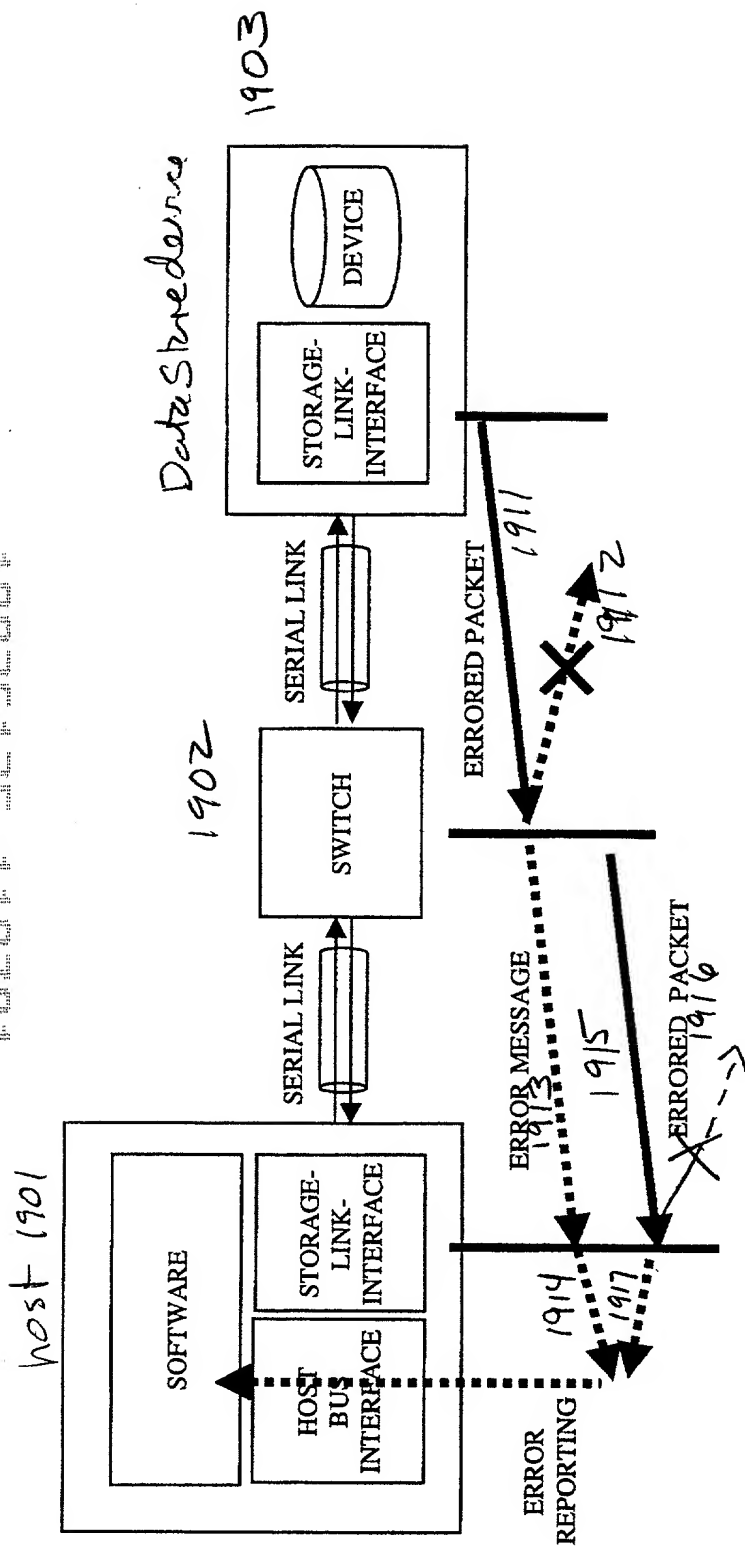
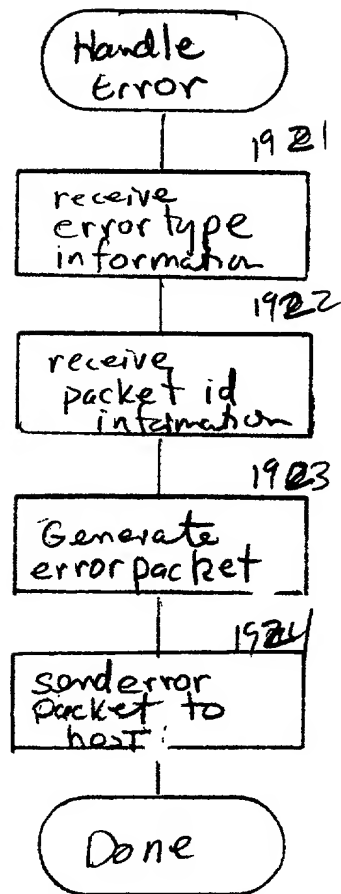


Fig 19B



19C

8b Code	9 bit symbol
0000 0000	101010101
0000 0001	101010100
0000 0010	101010111
⋮	
0101 0101	001010101
⋮	
0111 0110	001110110
0111 0111	100100010
⋮	
1111 1111	110101010

Fig 20



102076 5473400

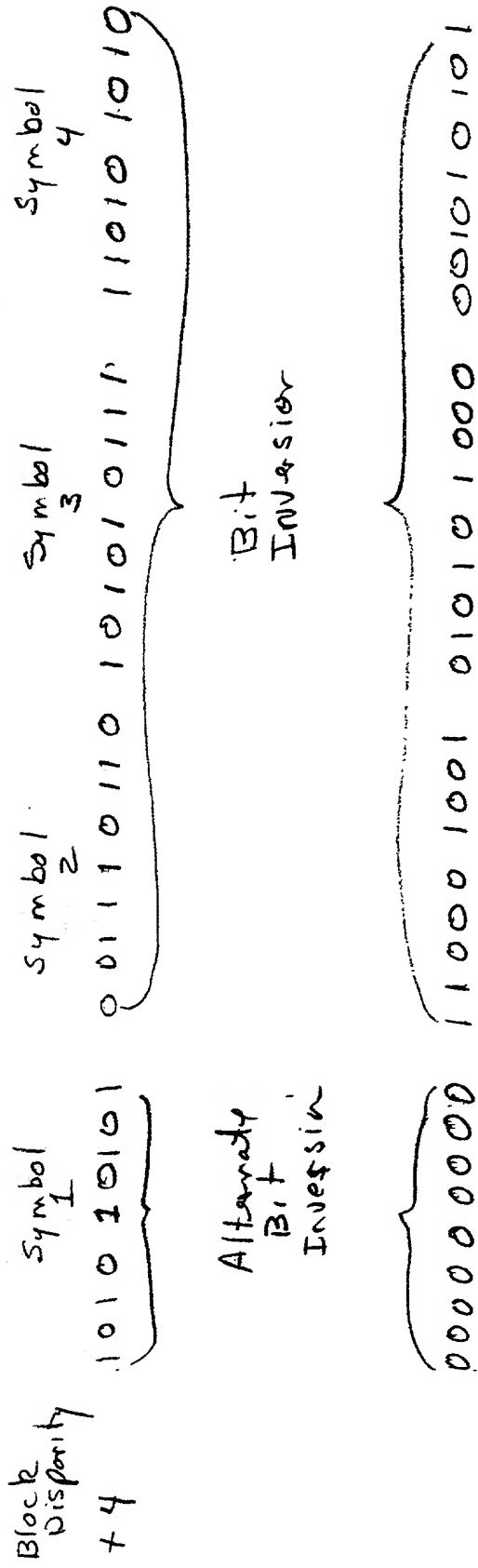


Fig 21A

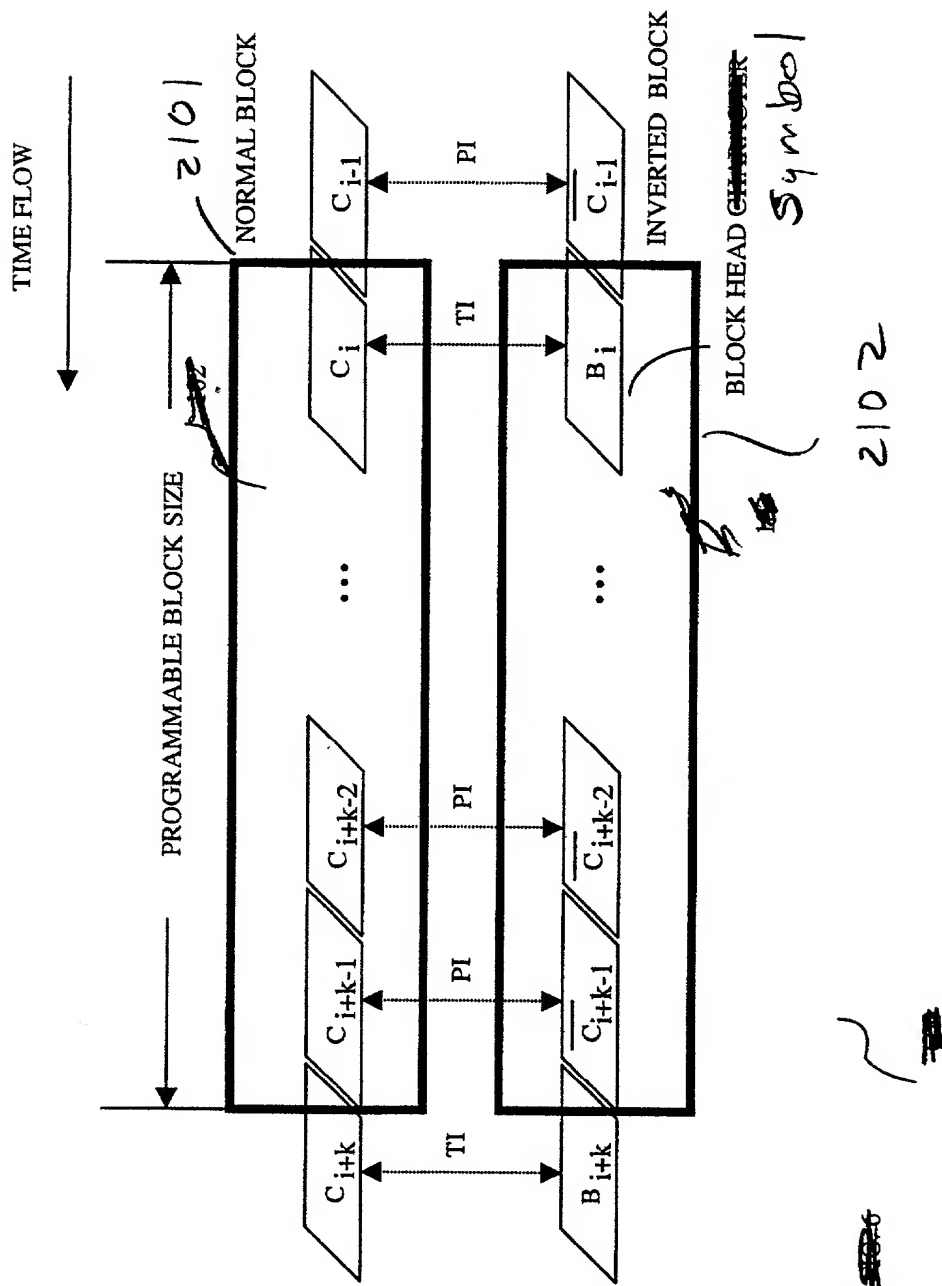


Fig 21B

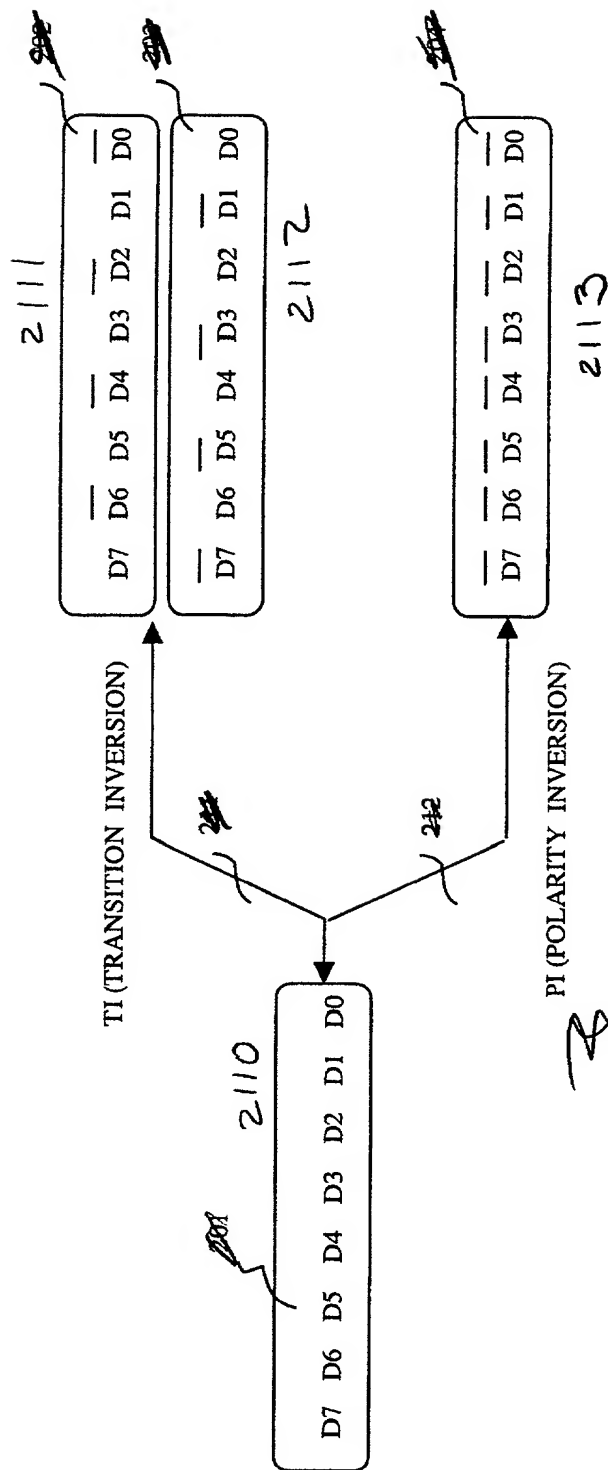


FIG. 21C

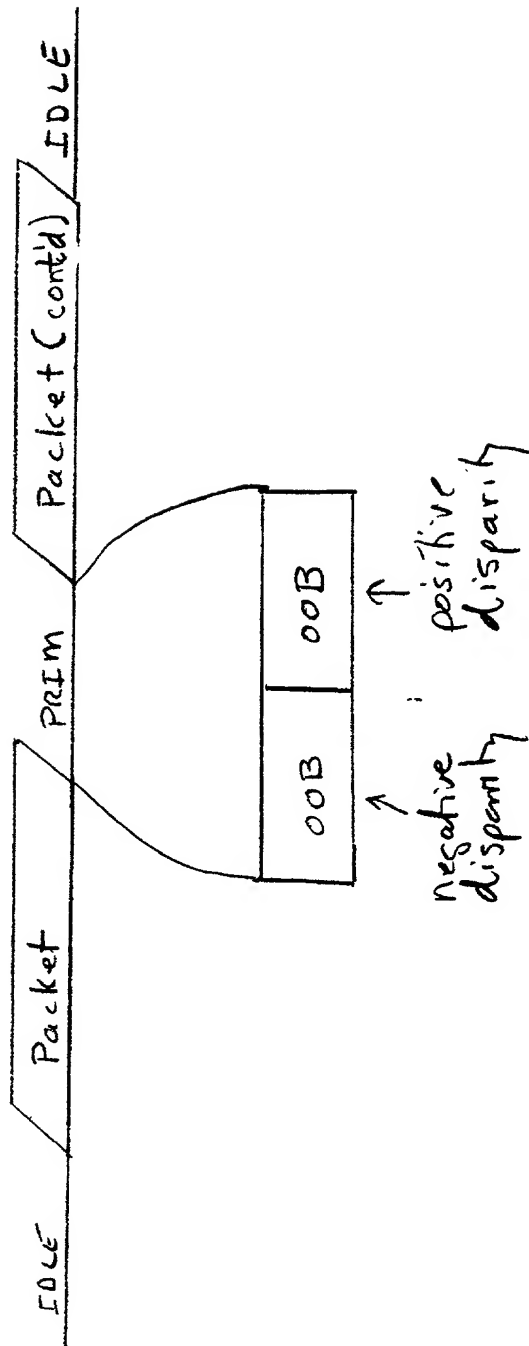


Fig 22

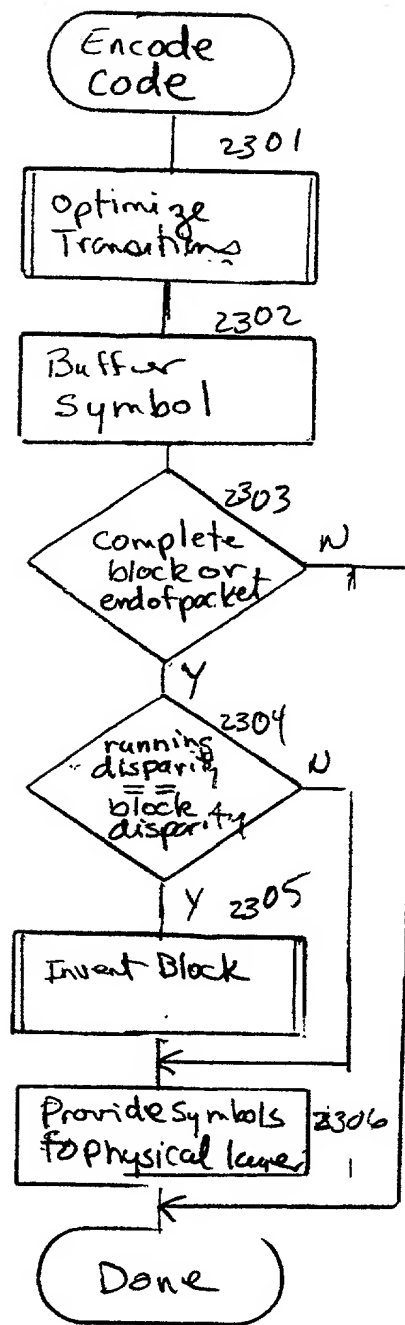


Fig 23

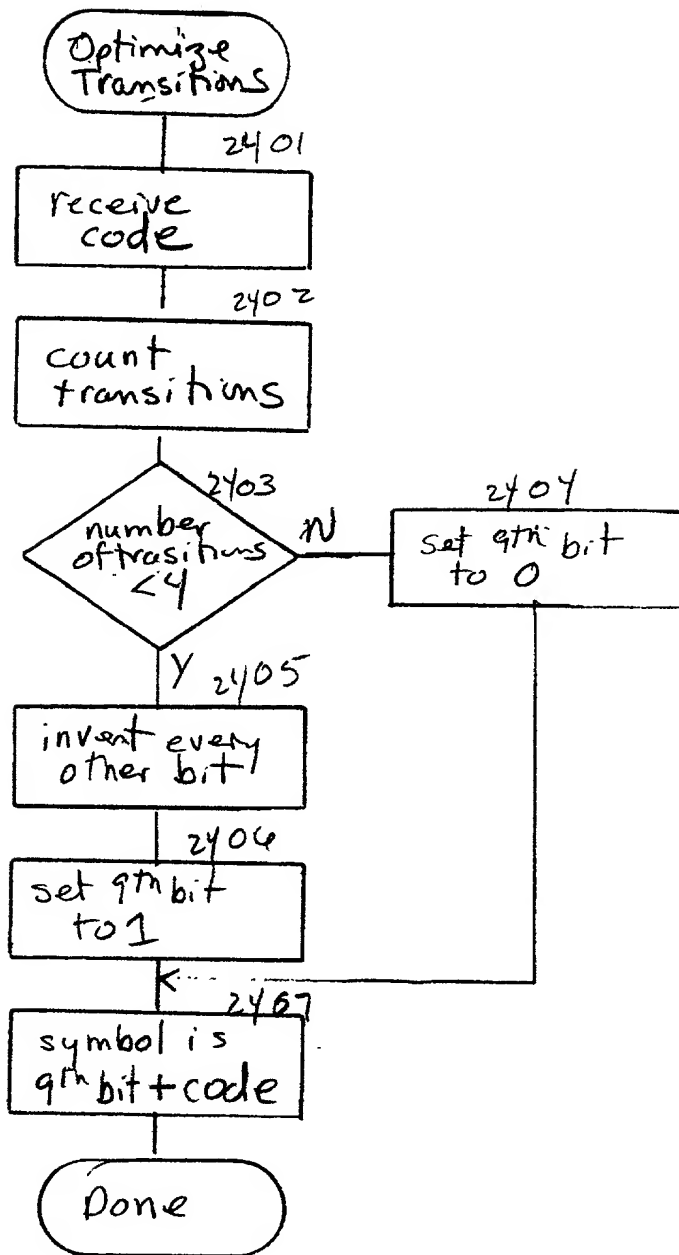


Fig 24

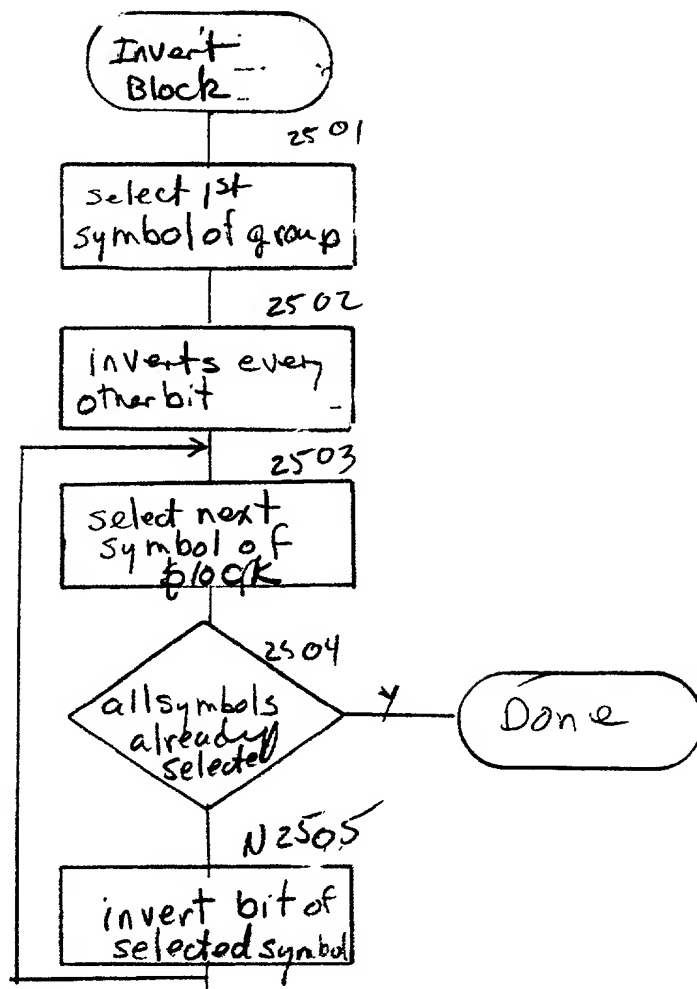


Fig 25

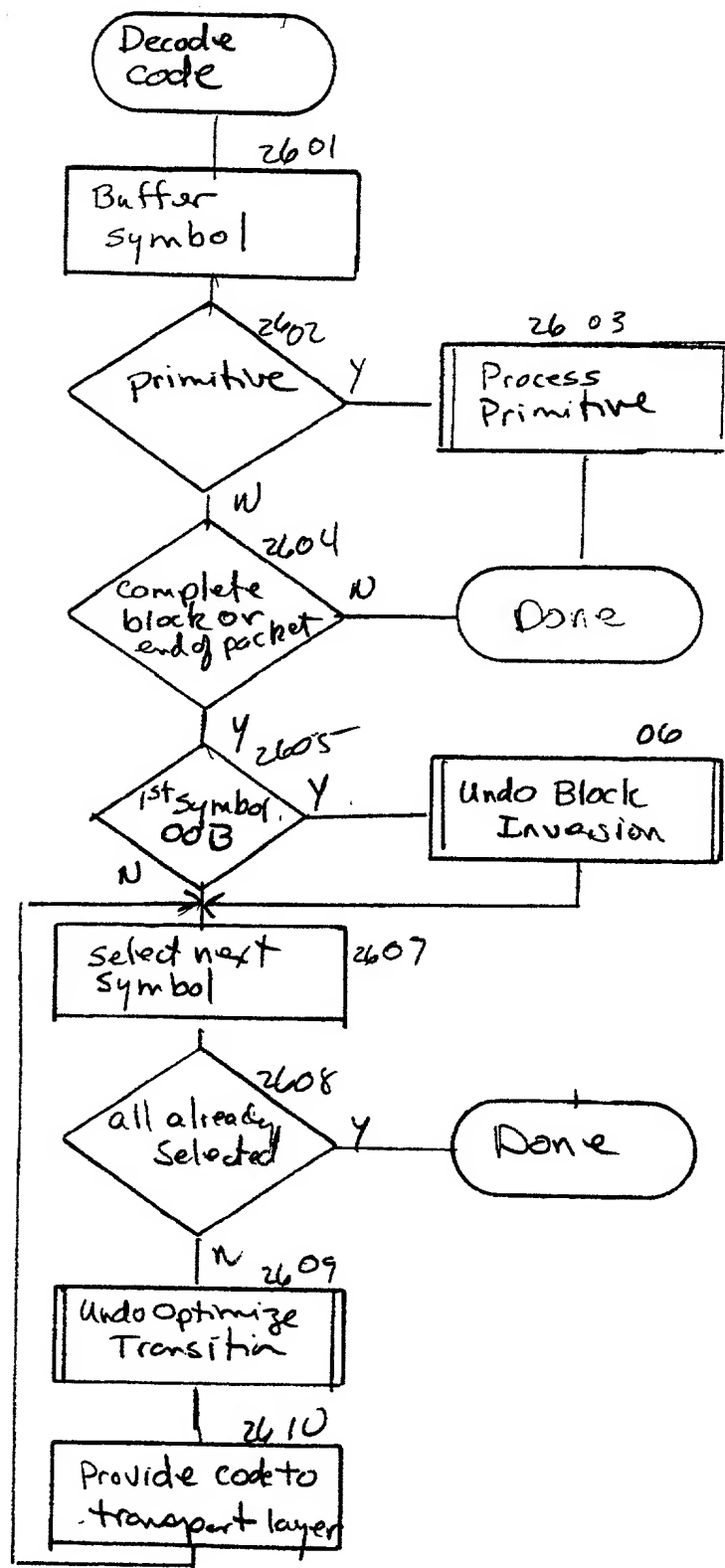


Fig 26



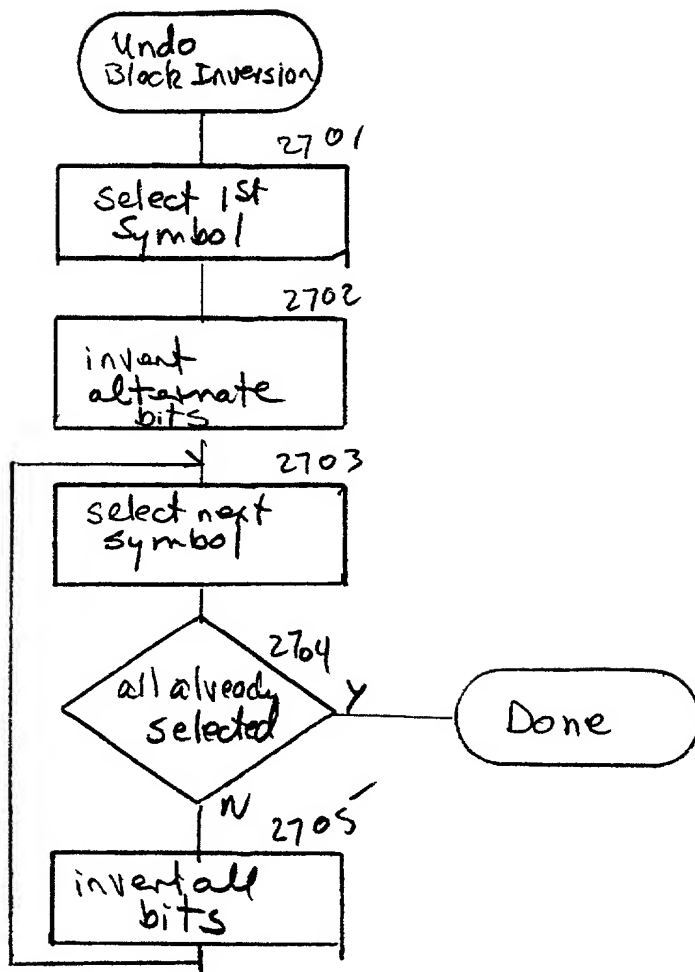


Fig 27

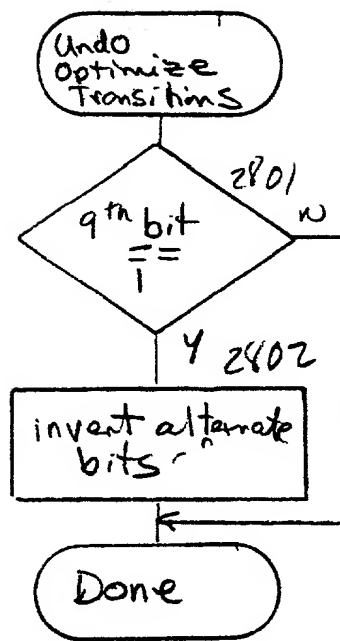


Fig 28

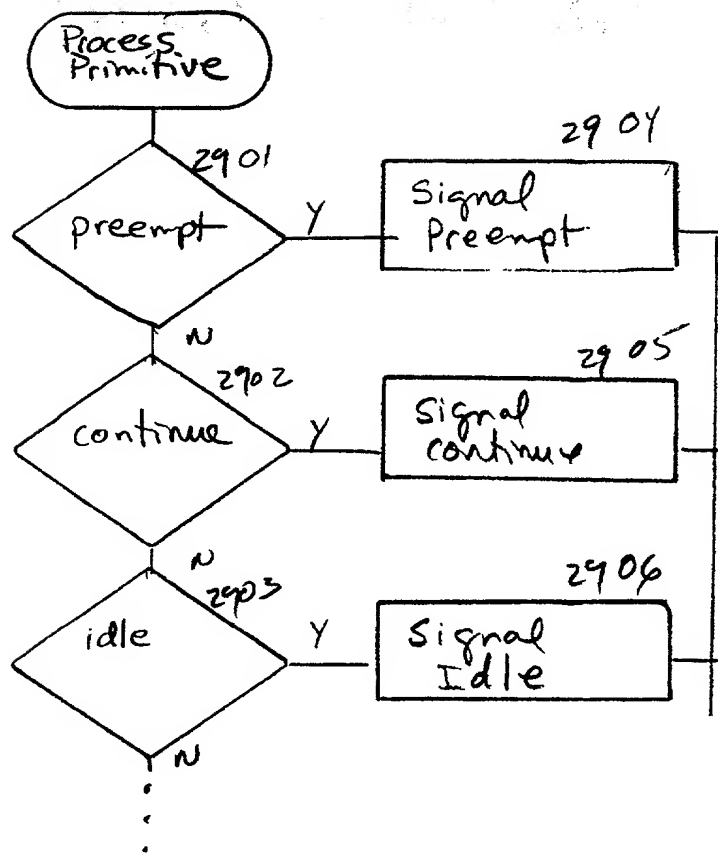


Fig 29

40036436 4004

# Multipoint Memory Device 3000

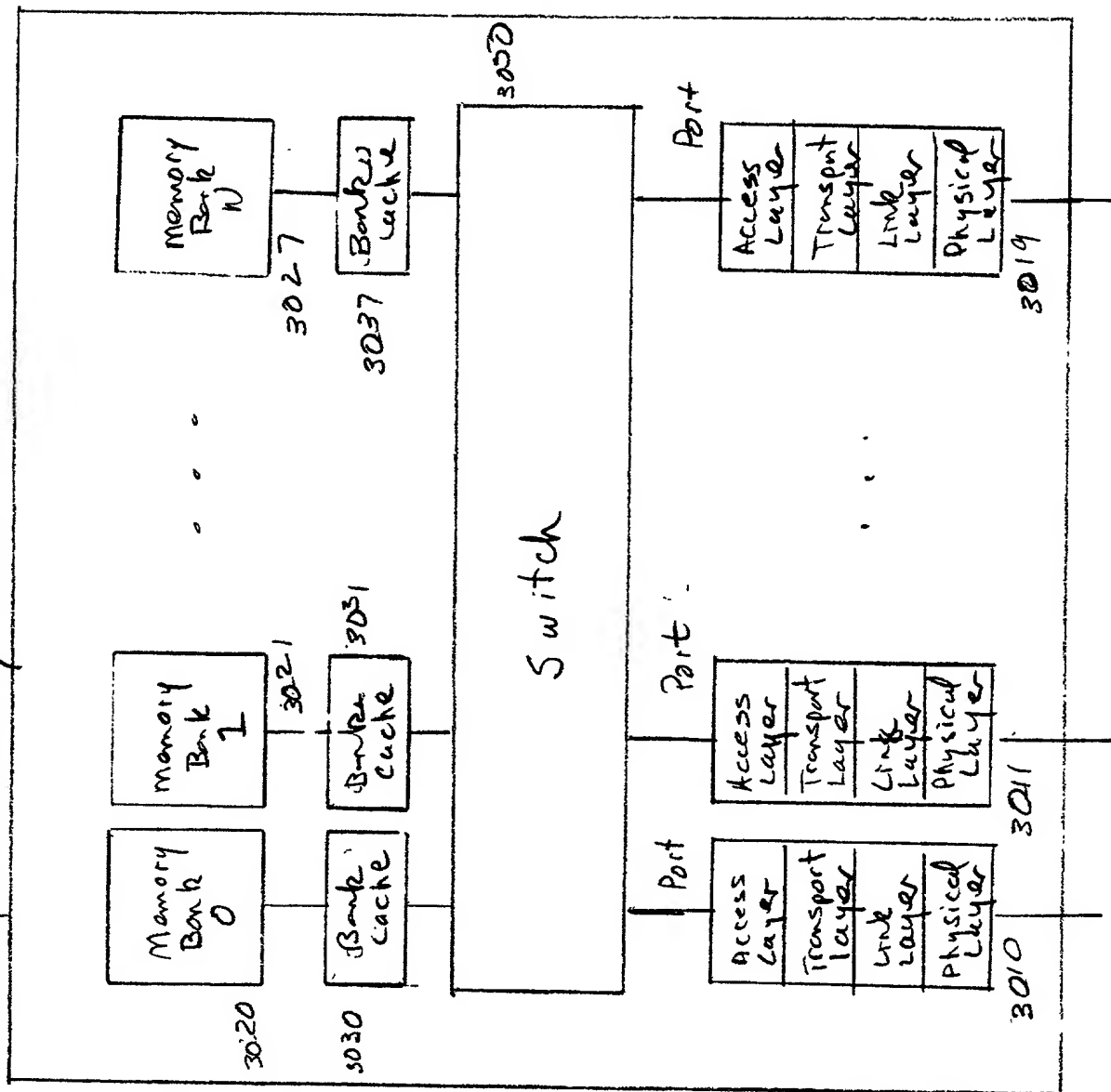
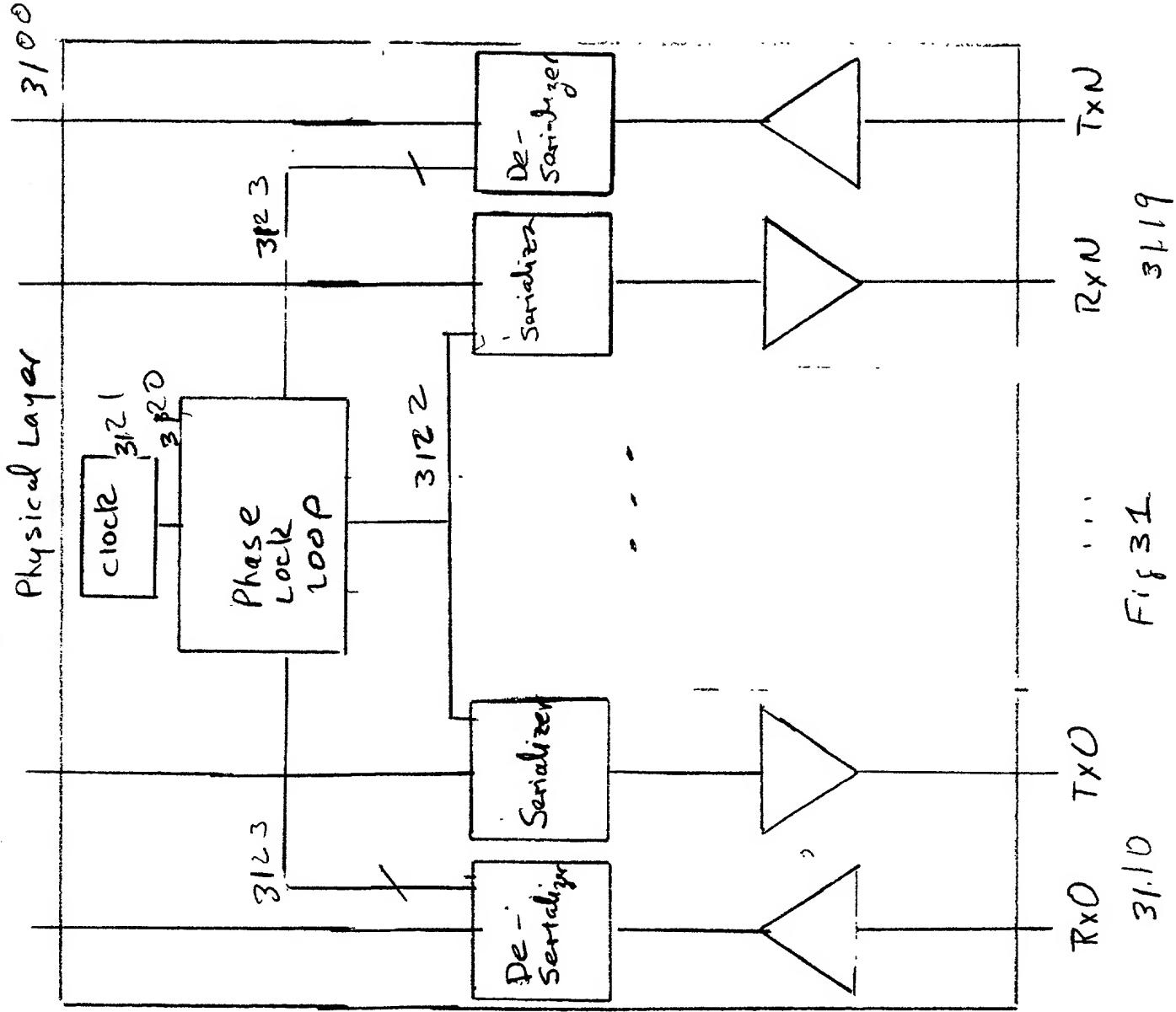


Fig 30



Input Queue 3201				Output Queue 3202			
Port	R/W	Address	Data	Valid	Port	Data	
3	R	1000		1	3	11...0	
4	W	4000	10...1	0			
3	W	1000	111...0	0			
3	R	2000		1	3	101...1	
					⋮		

Fig 32

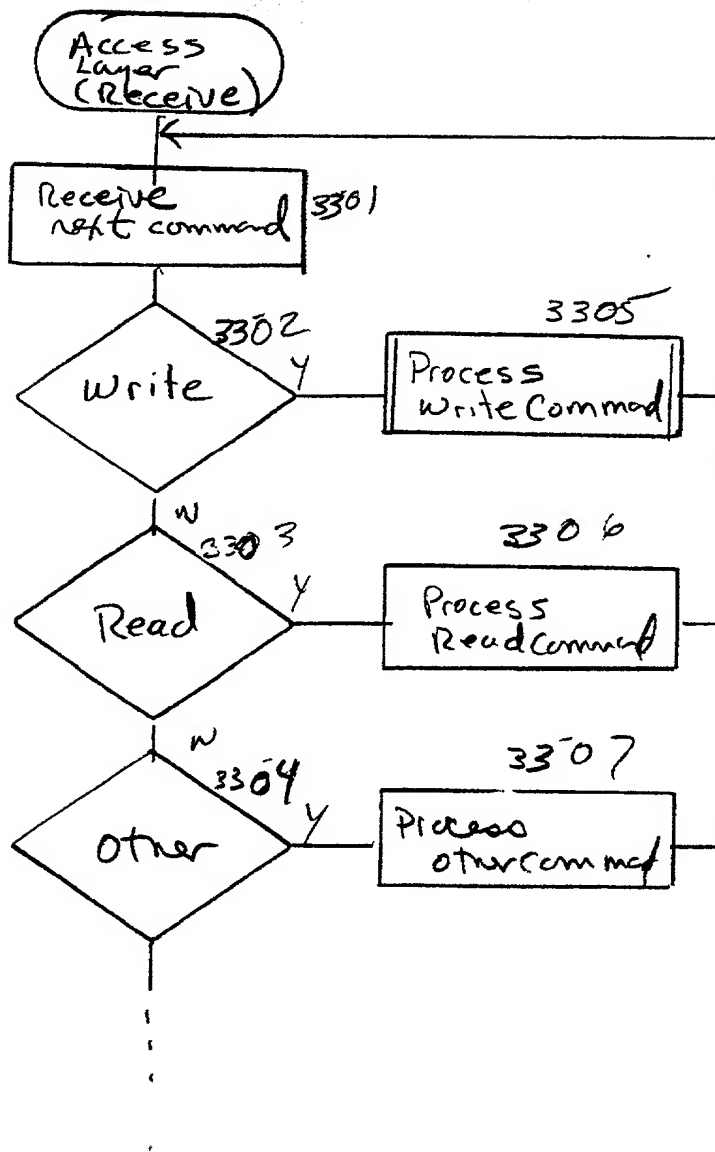


Fig 33

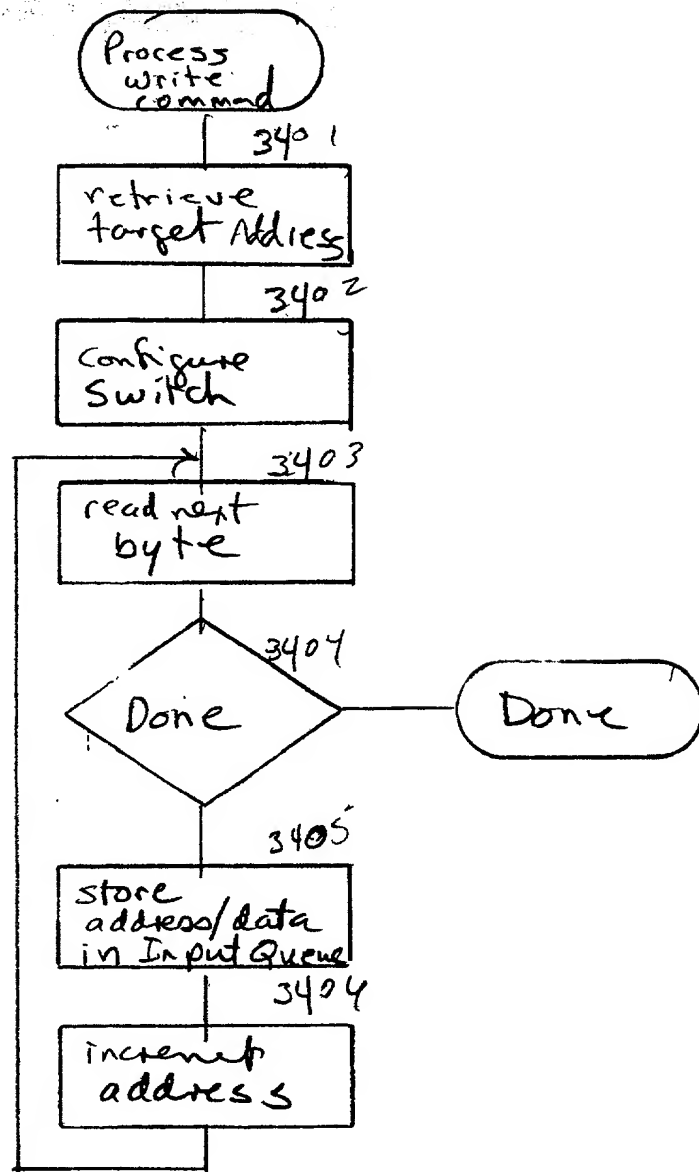


Fig 34



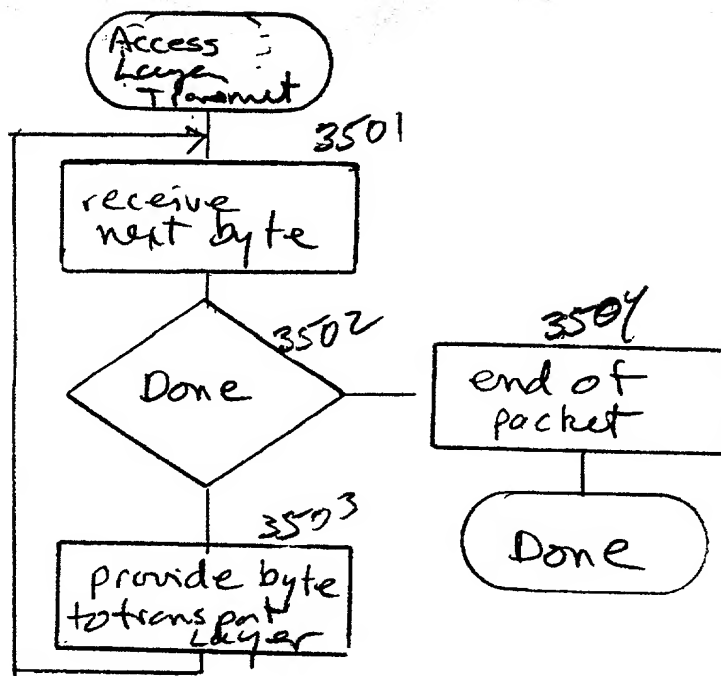


Fig 35

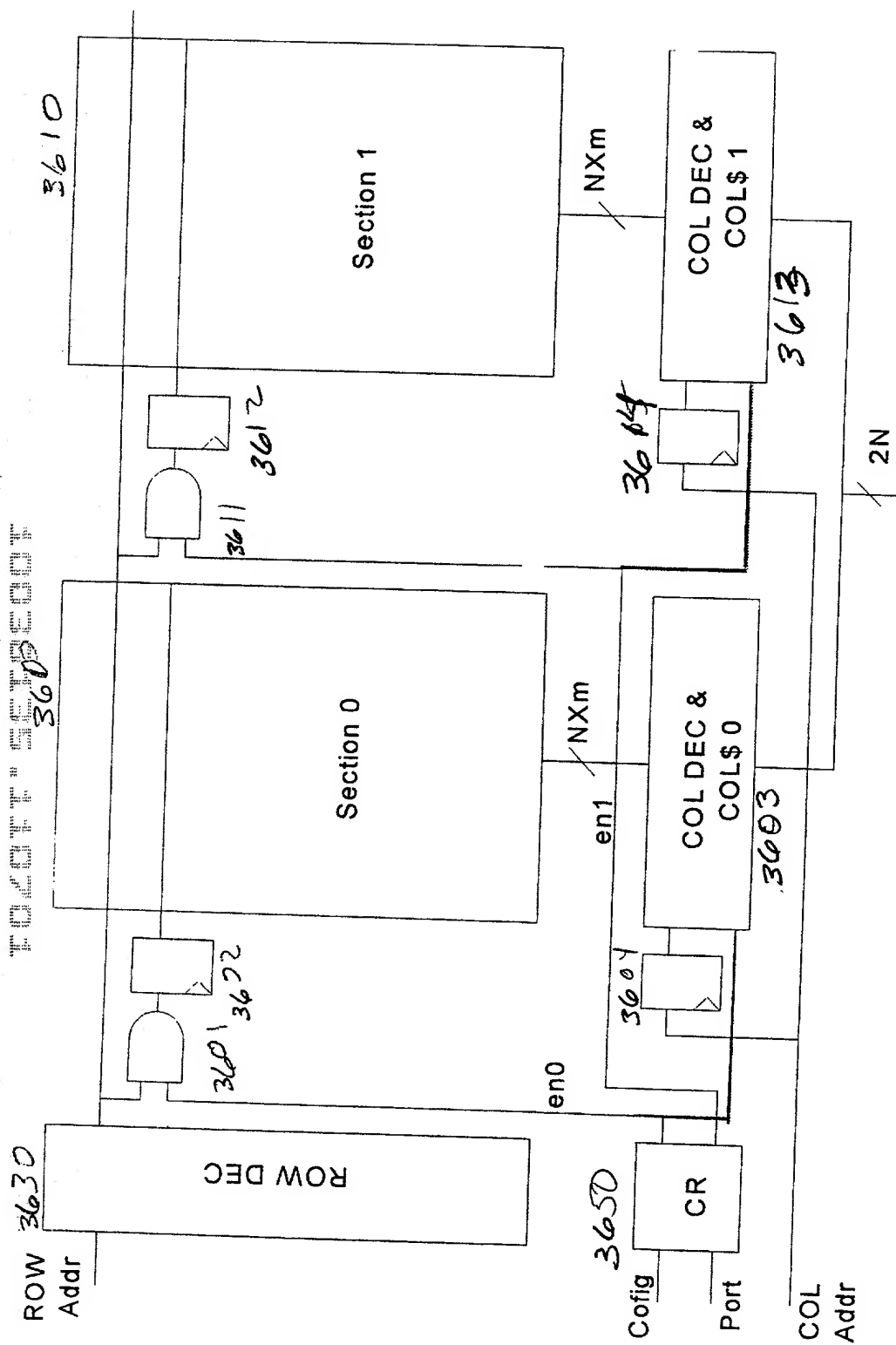
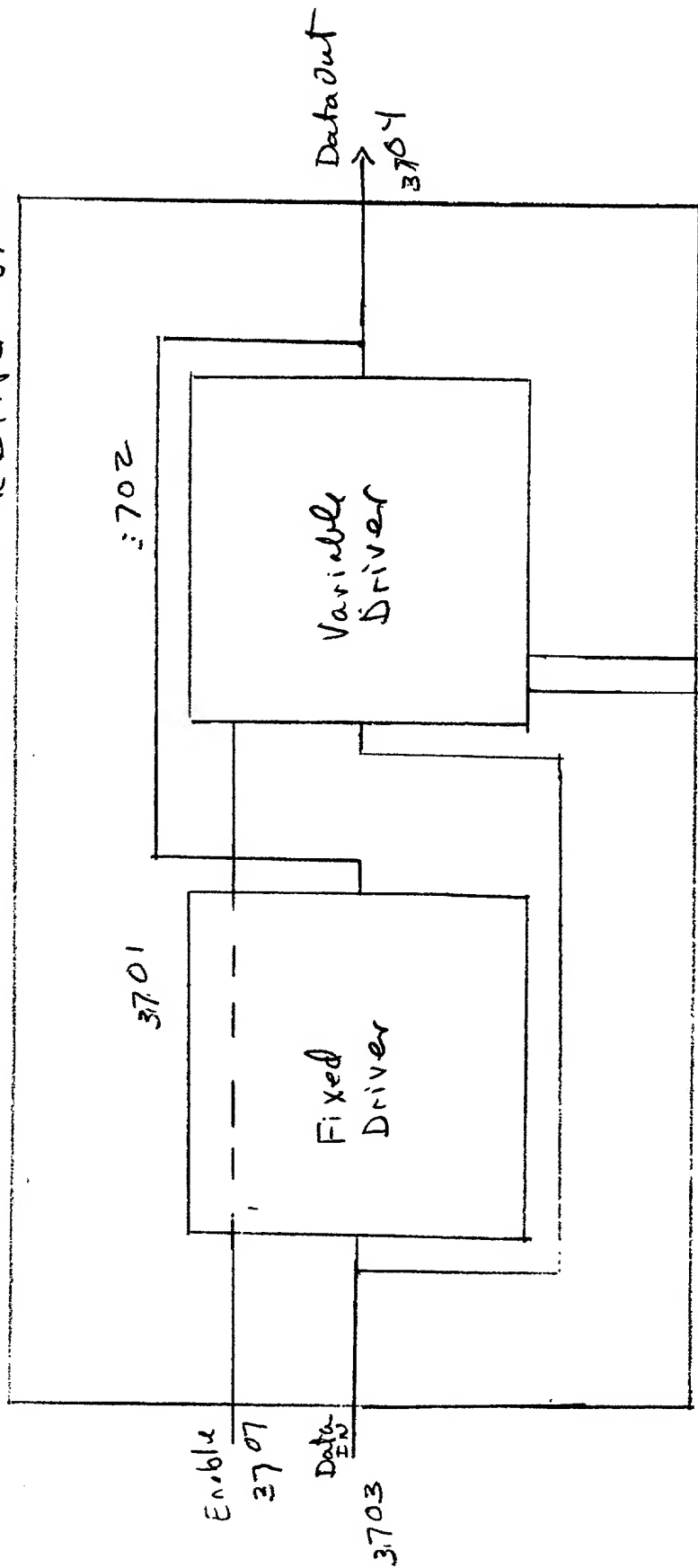


FIG. 36

# Line Driver 3700



Variable Driver

$$\begin{cases} RD^+ \wedge \overline{DataIn} = \text{pull down} \\ RD^- \wedge DataIn = \text{pull up} \end{cases}$$

Fig 37A

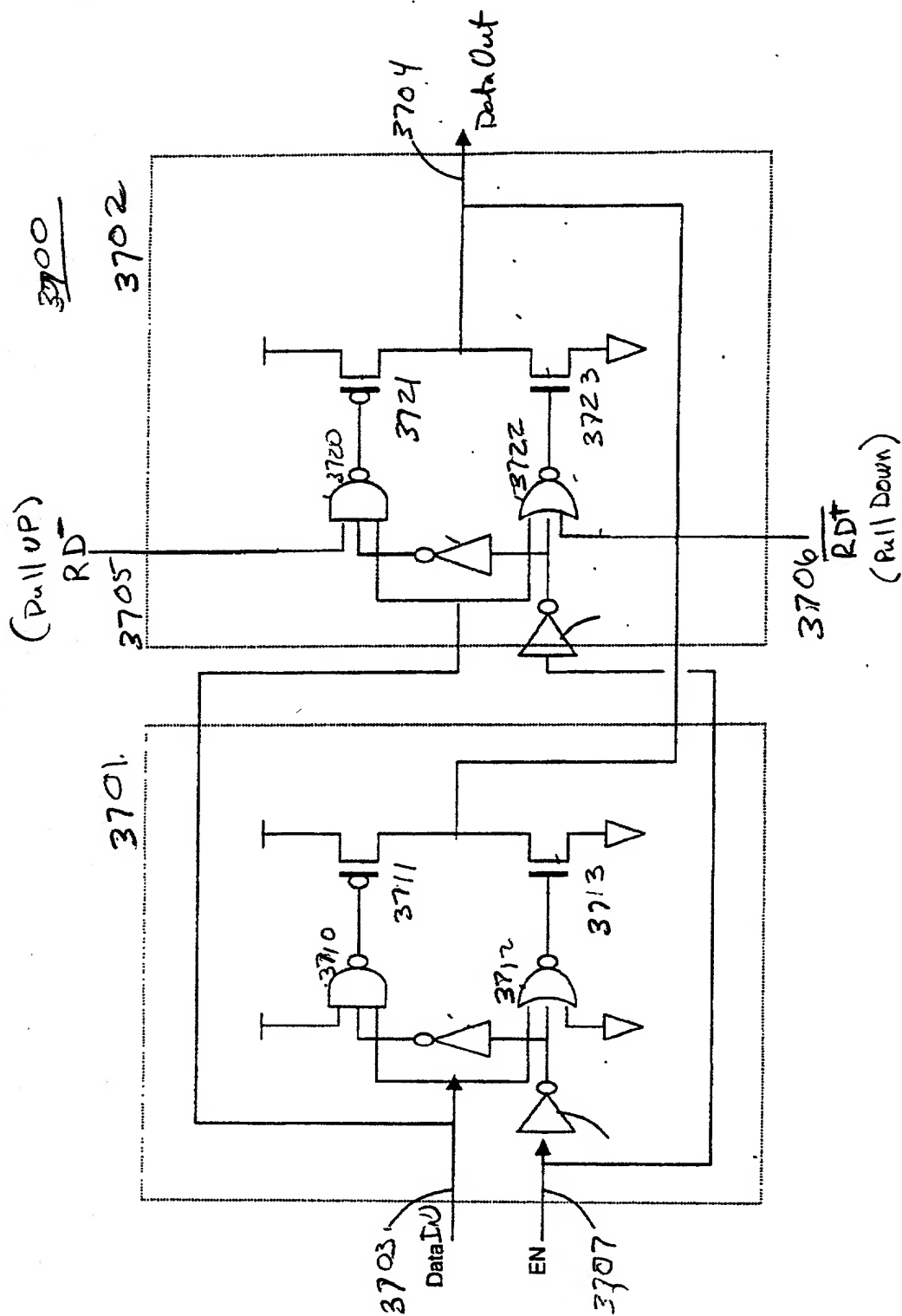
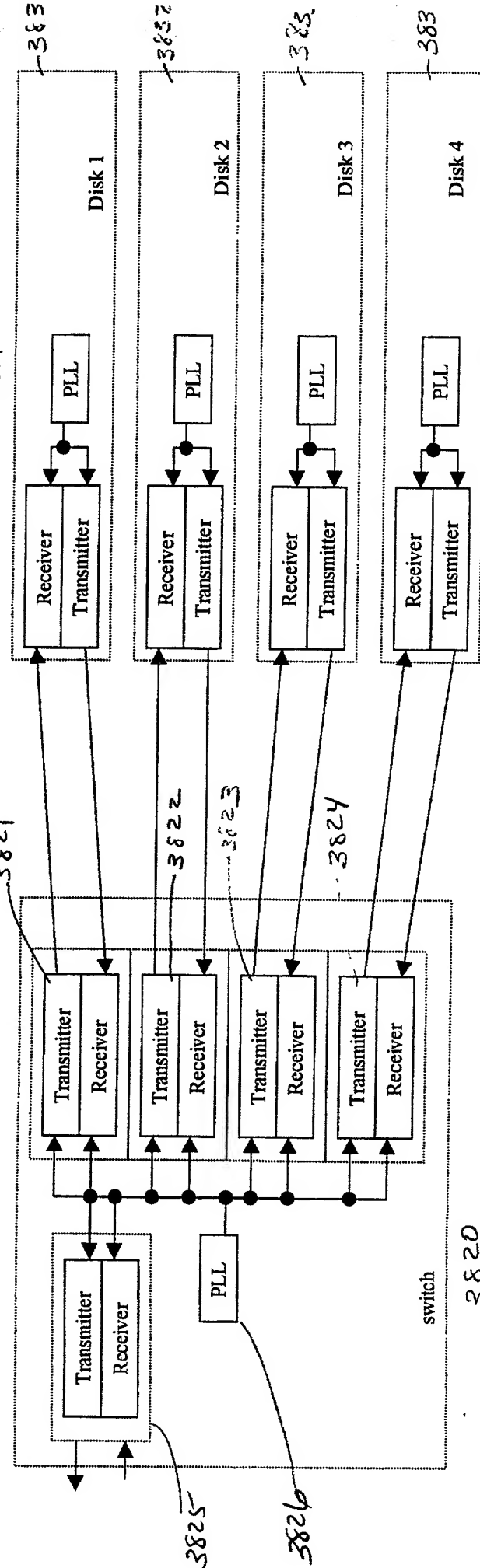
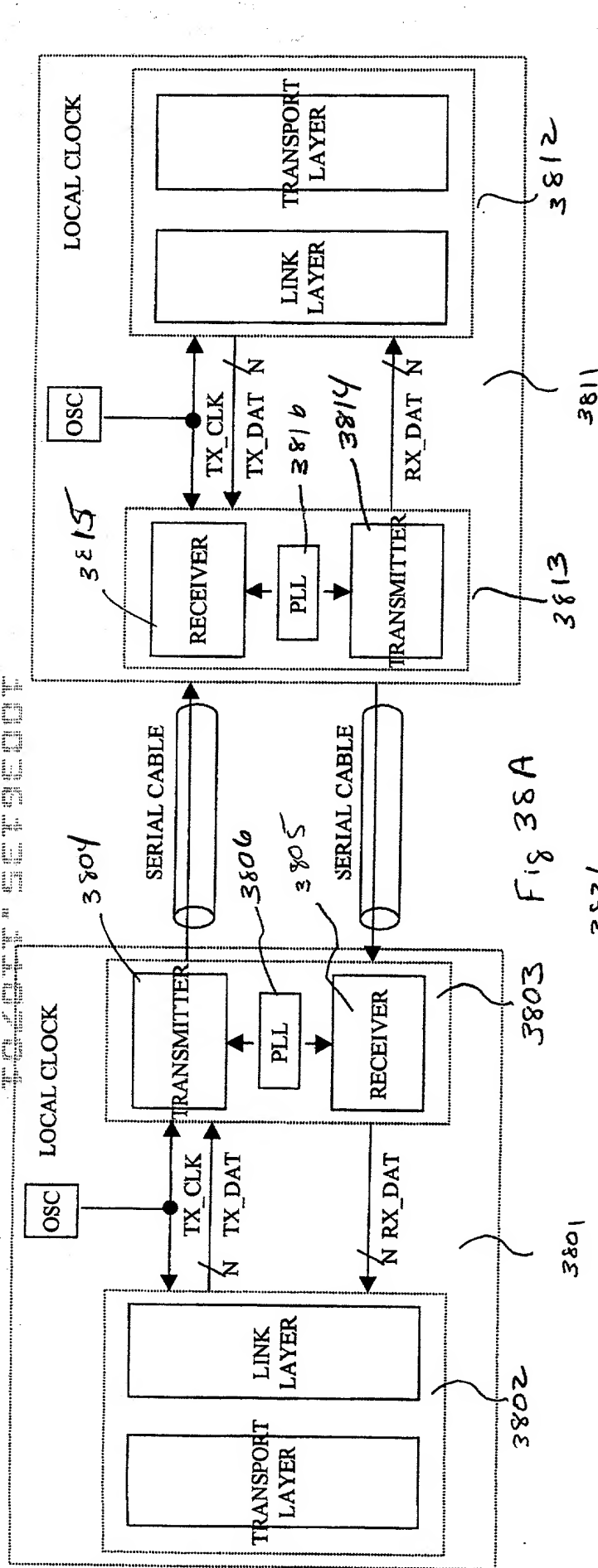


Fig 37B



3910

3921

3920

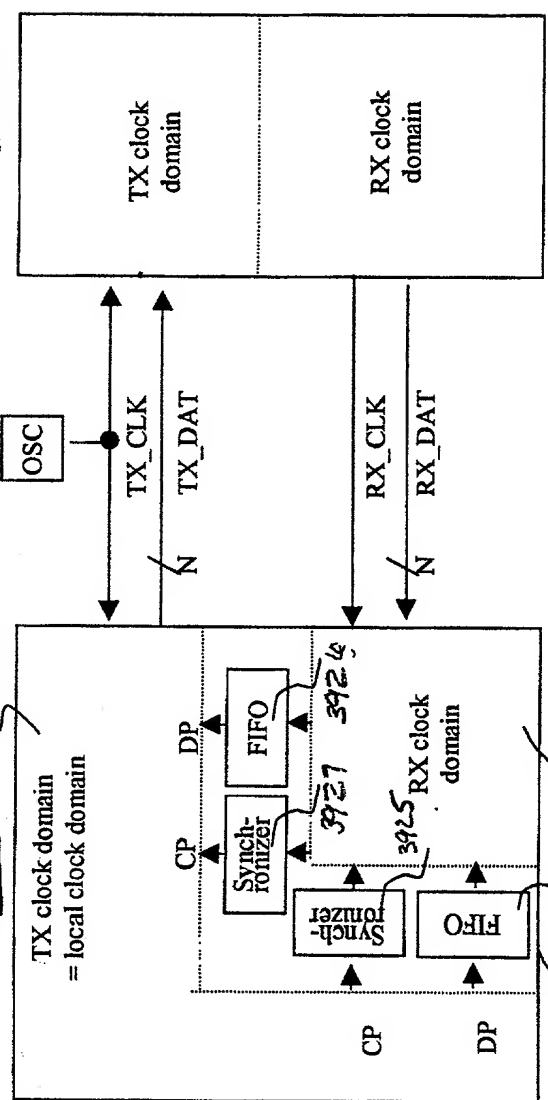


Fig 39A

3950

3960

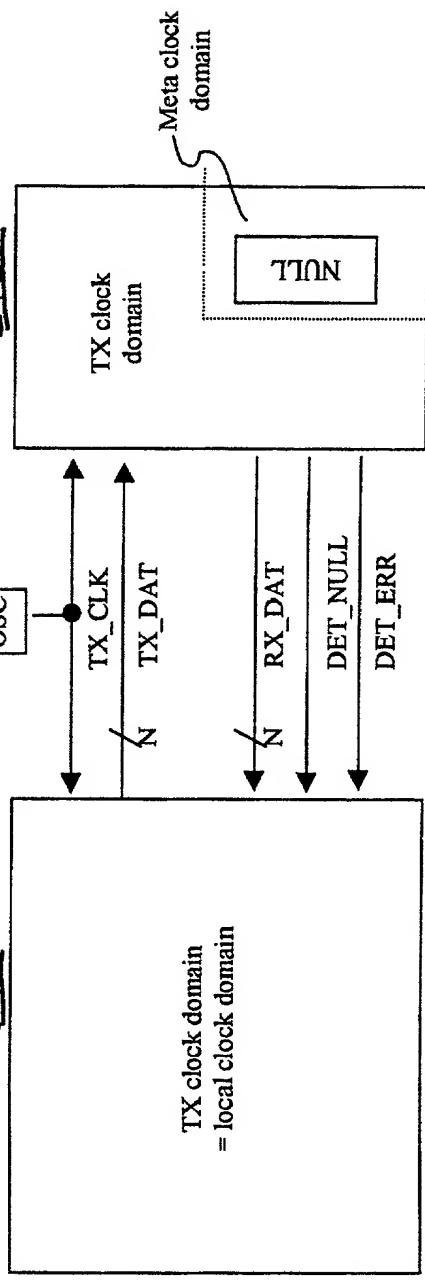


Fig 39B

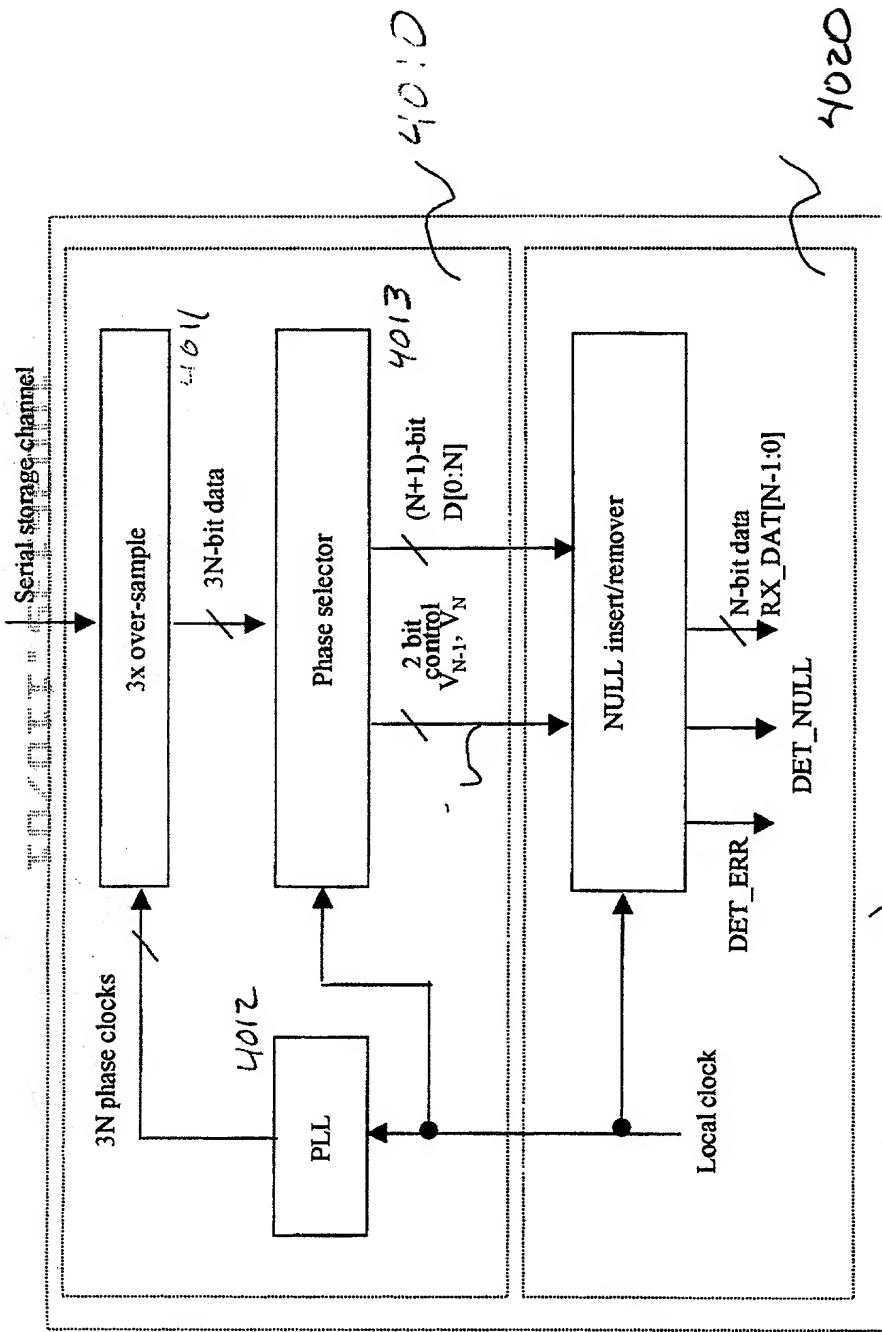


Fig 40

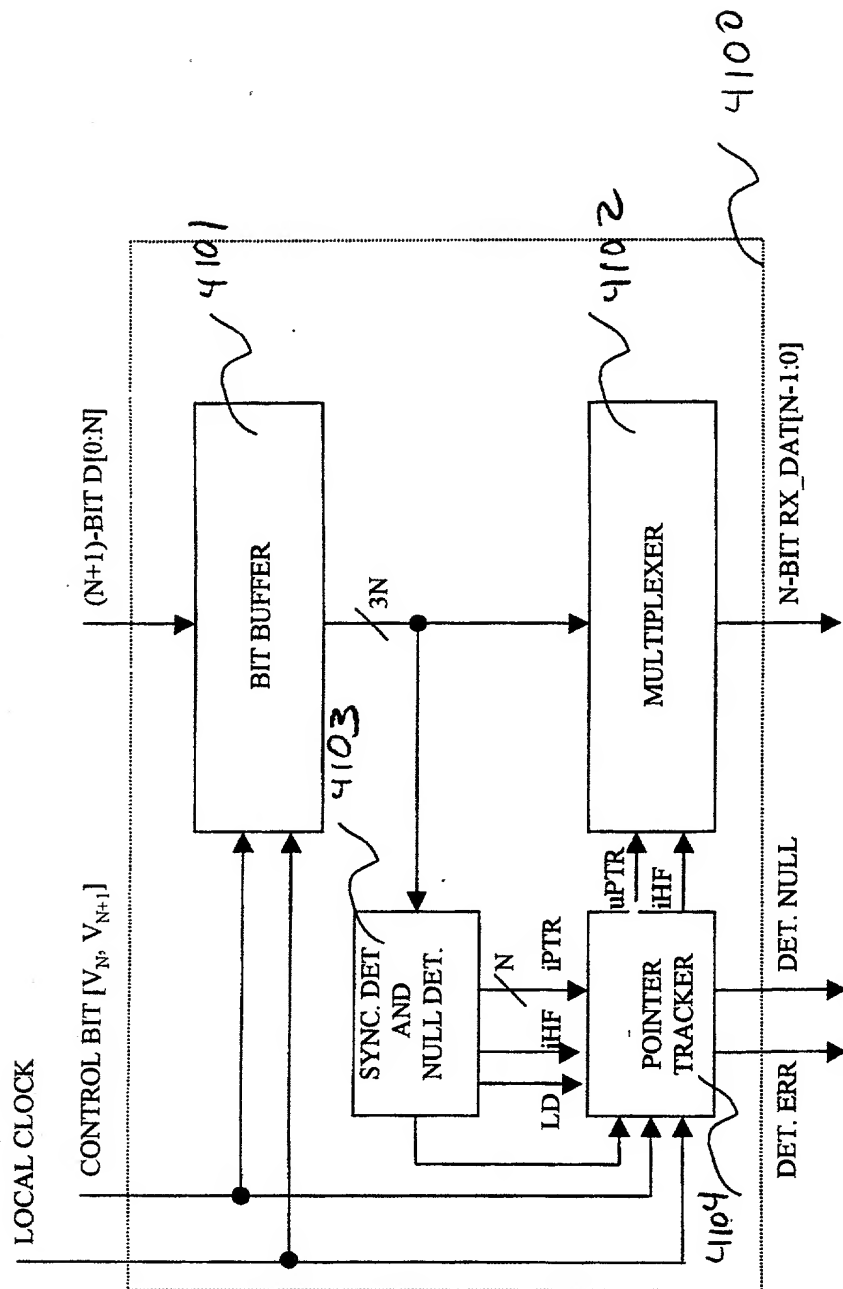


Fig 41



$[V_{N-1}, V_N] = [1, 0]$

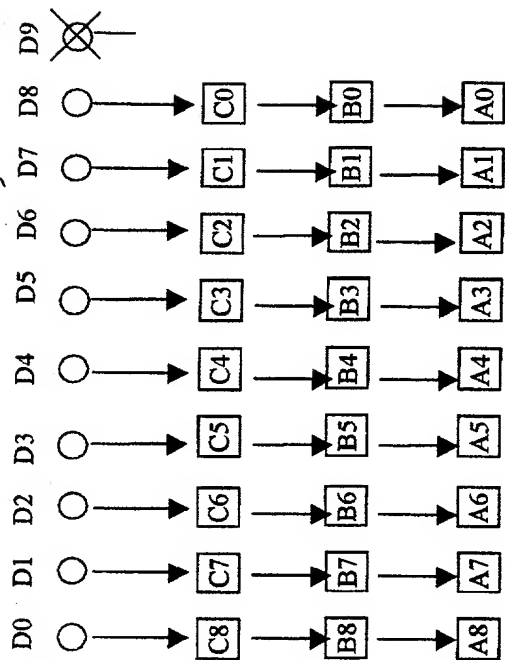


Fig 42A

$[V_{N-1}, V_N] = [0, 0]$

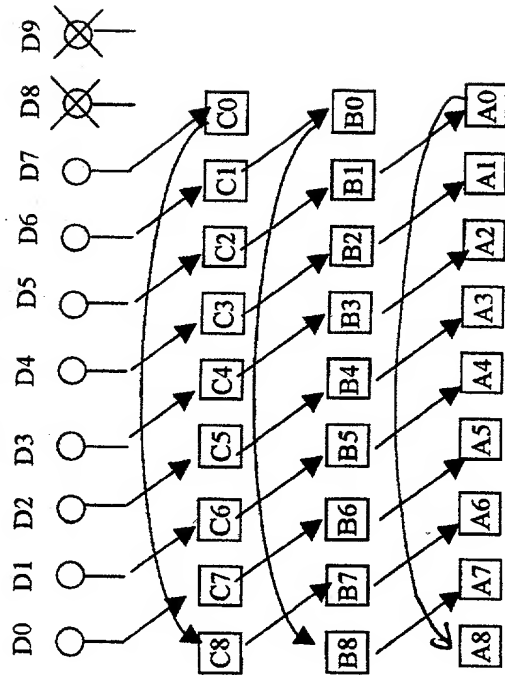


Fig 42B

$$[V_{N-1}, V_N] = [1, 1]$$

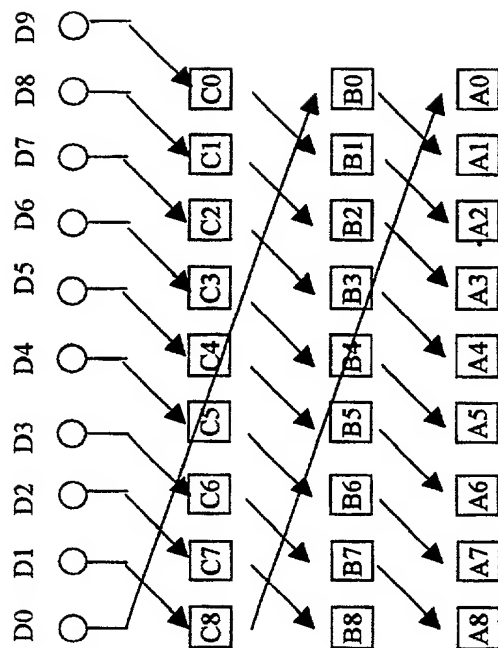


Fig 42c

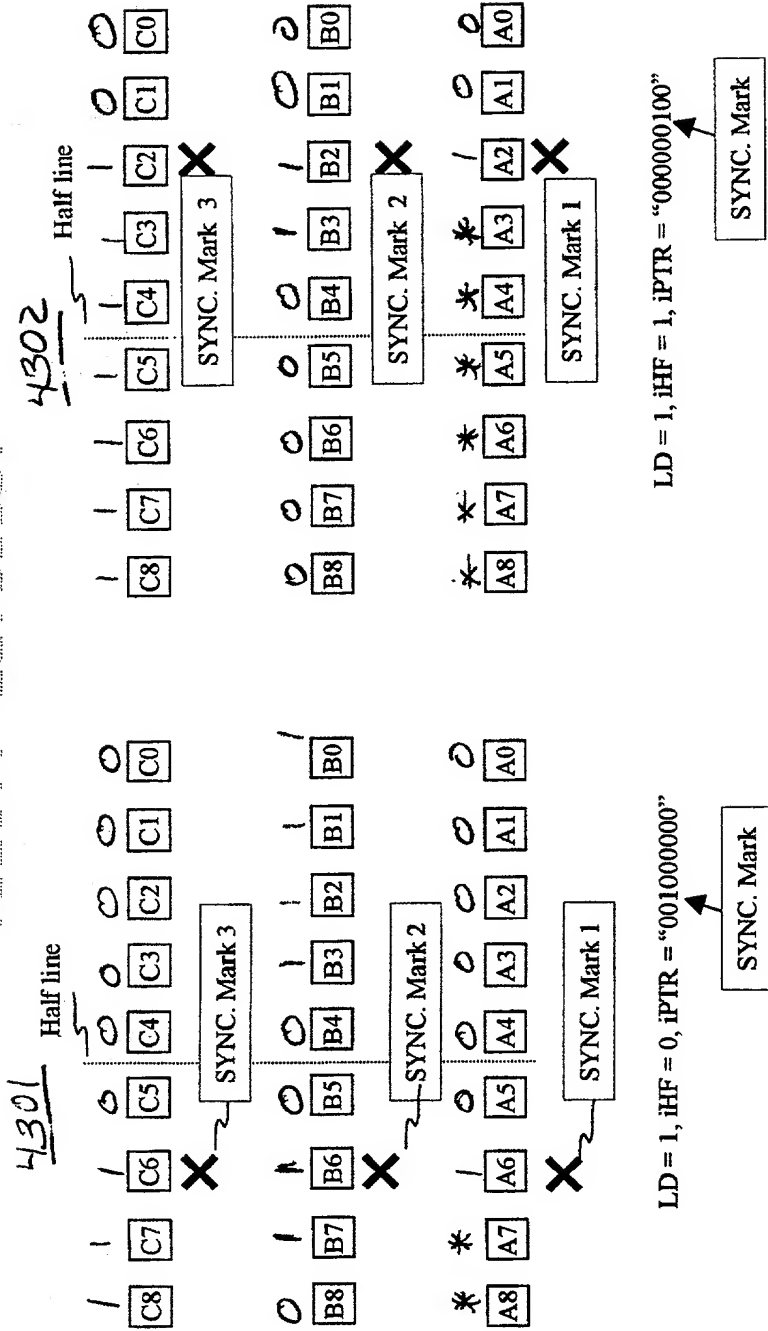
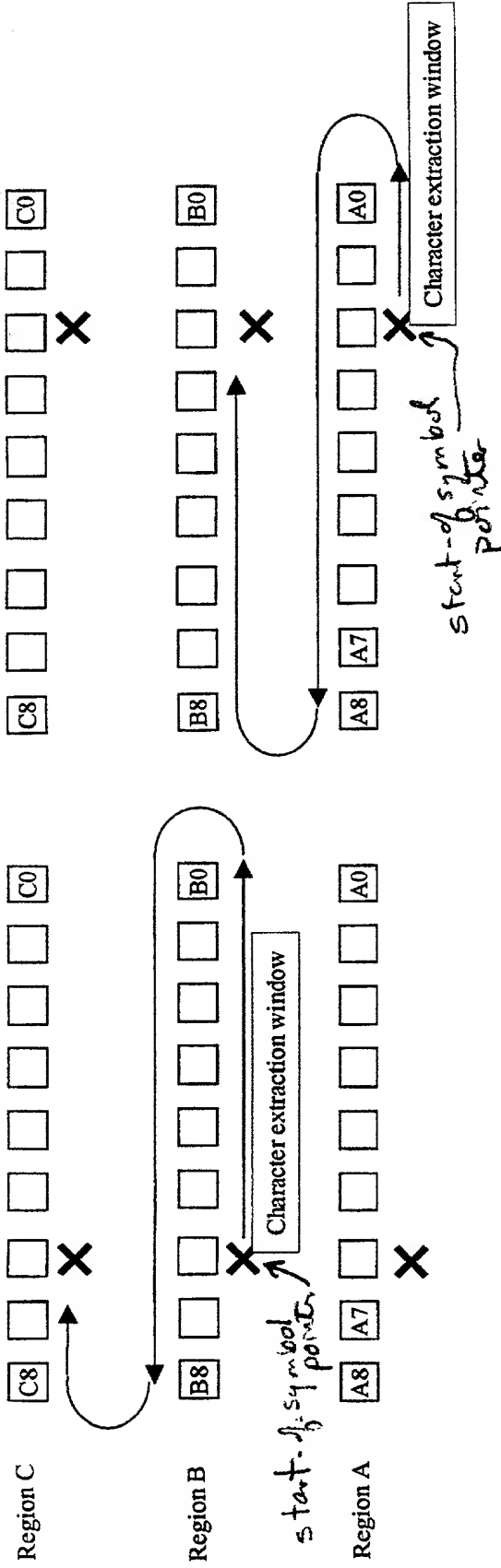


Fig. 43



LD = 1, iHF = 0, iPTR = "001000000"

LD = 1, iHF = 1, iPTR = "000000100"

Fig 44

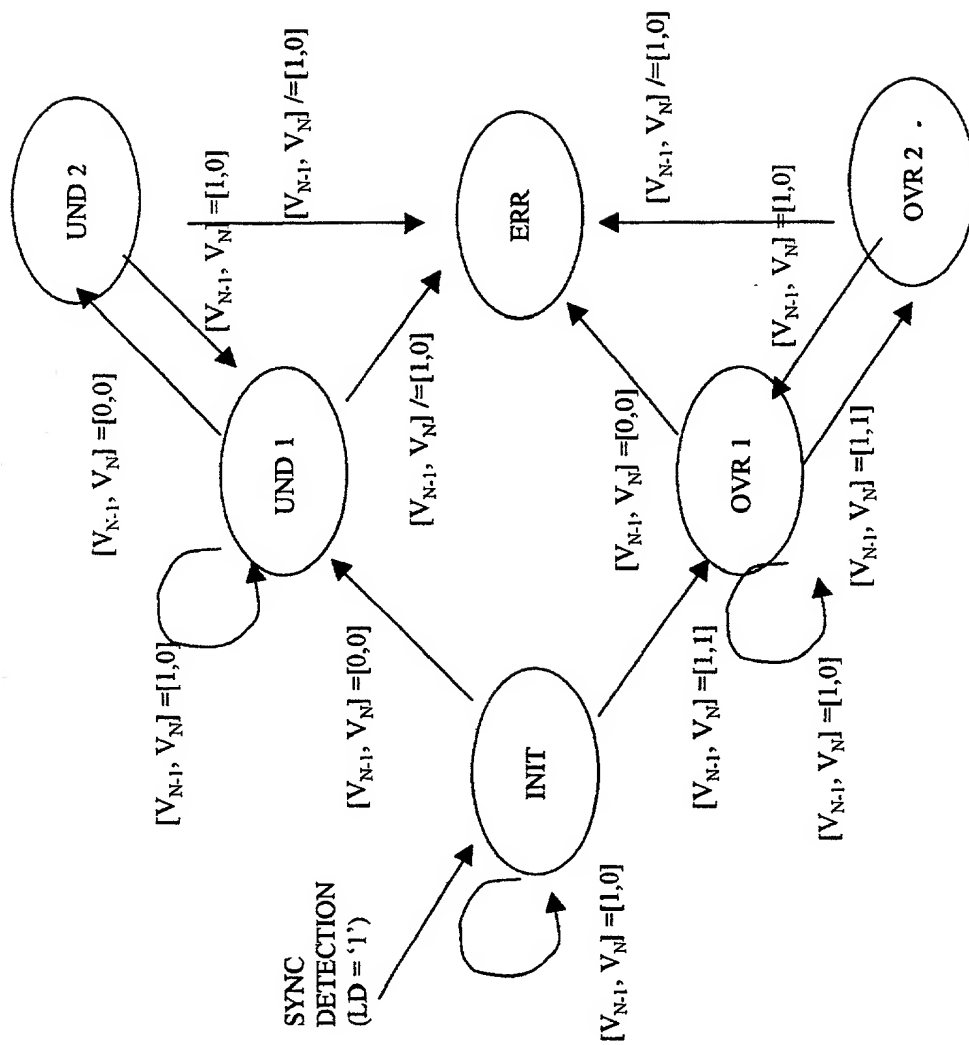


Fig 45

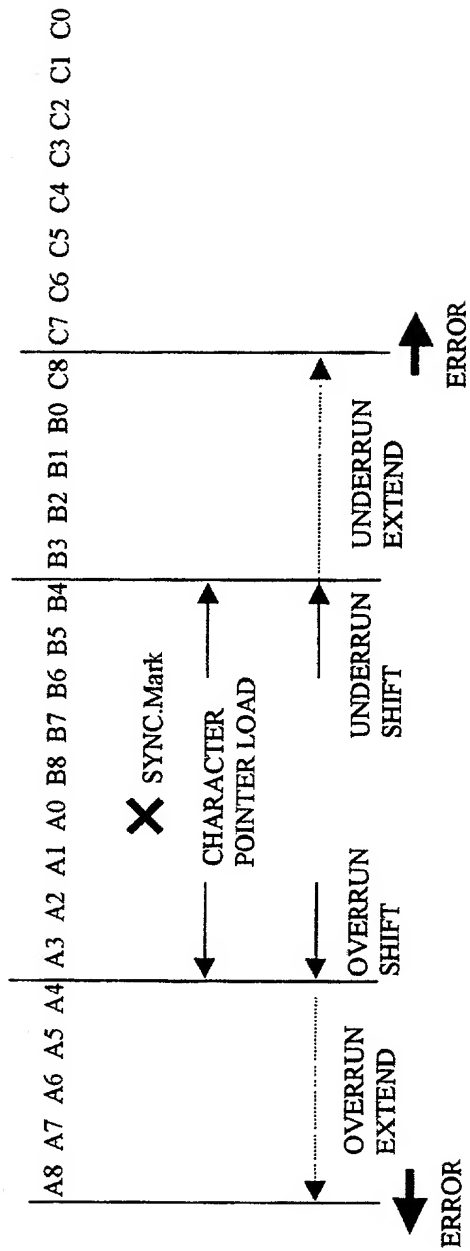


Fig 46

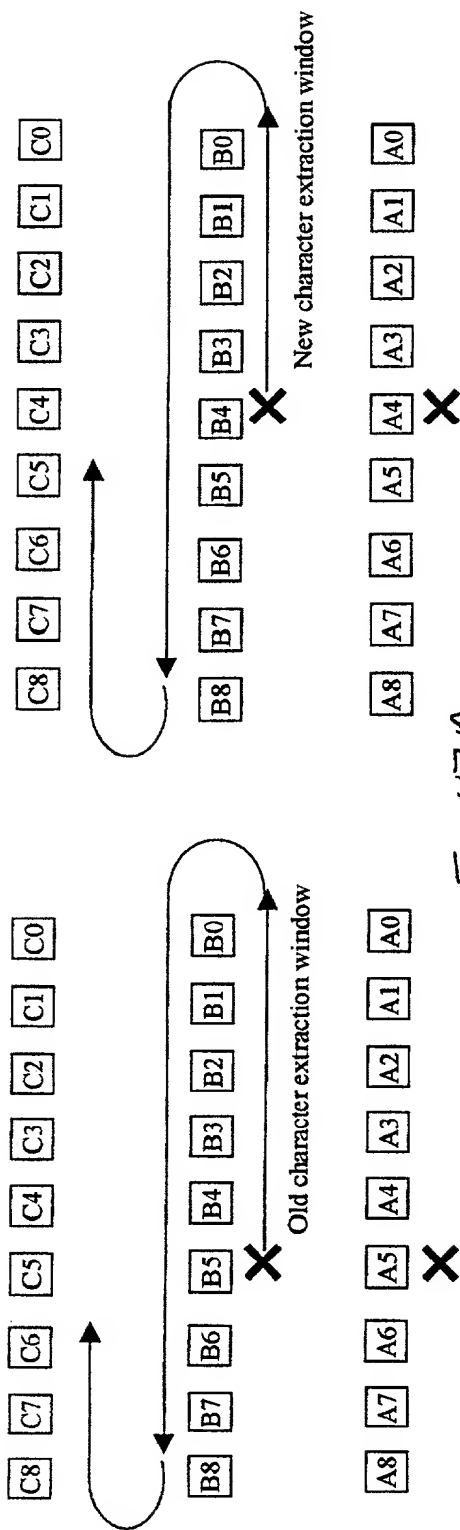


Fig 47A

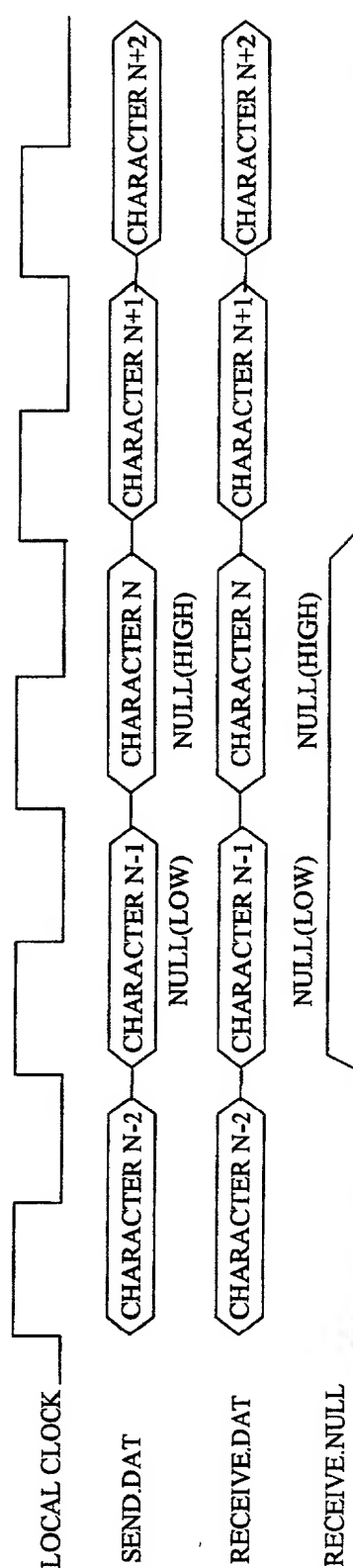


Fig 47B



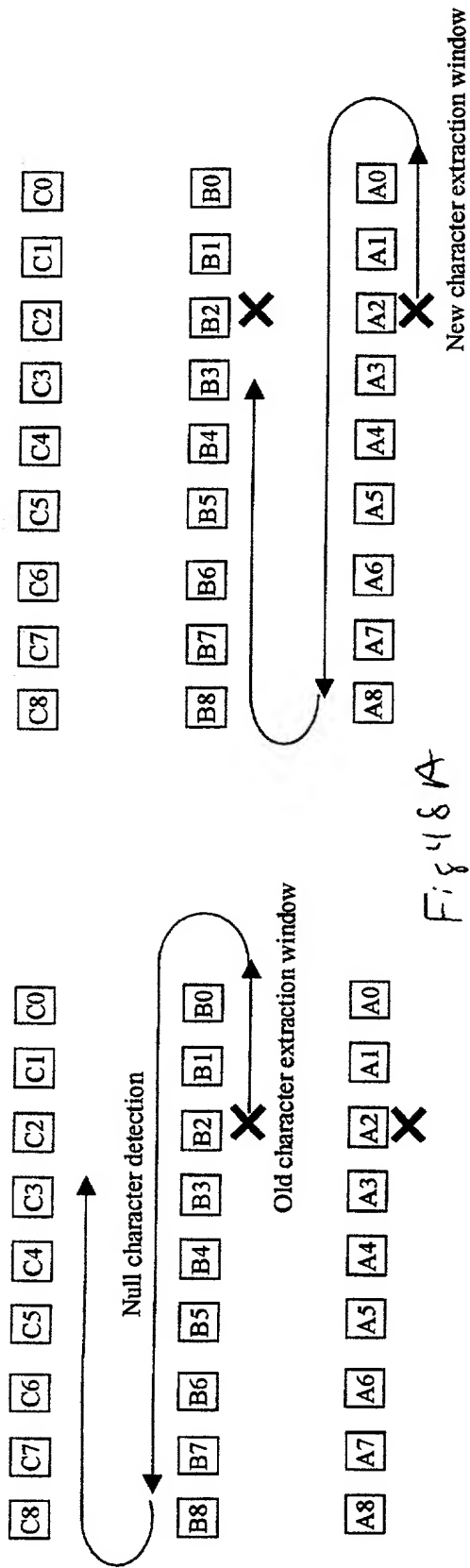


Fig 48A

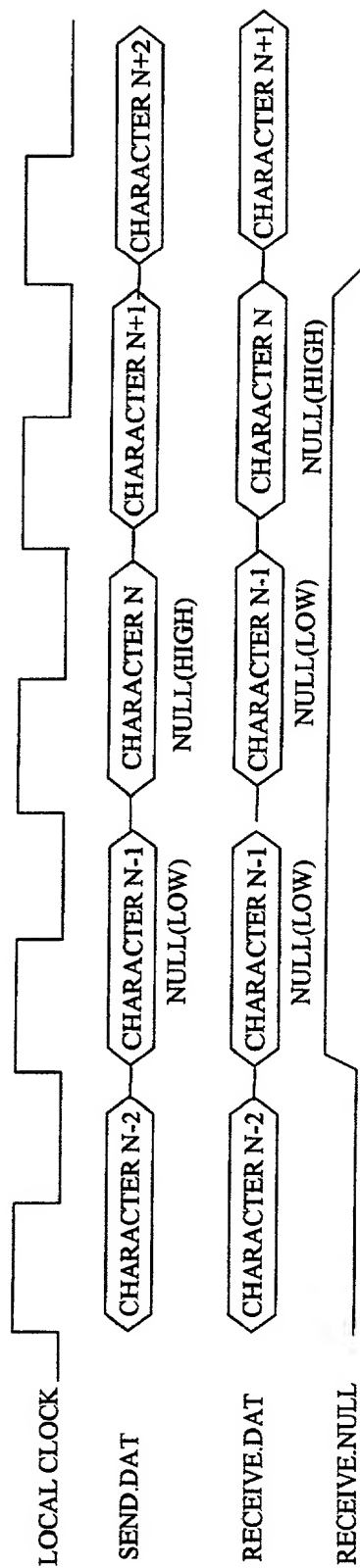


Fig 48B

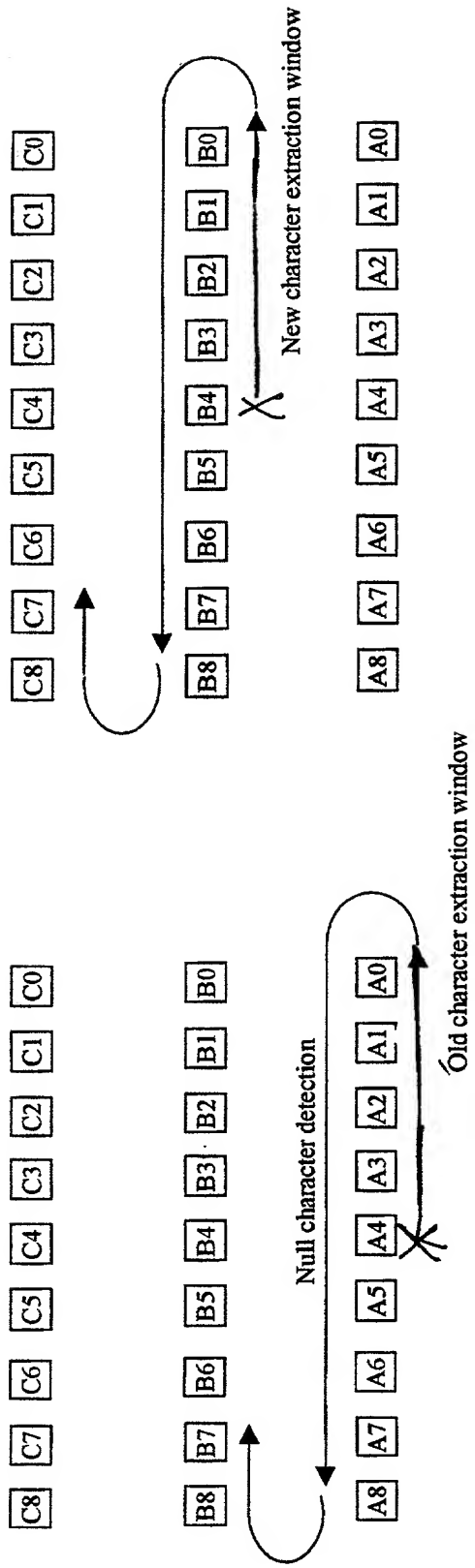


Fig. 49A

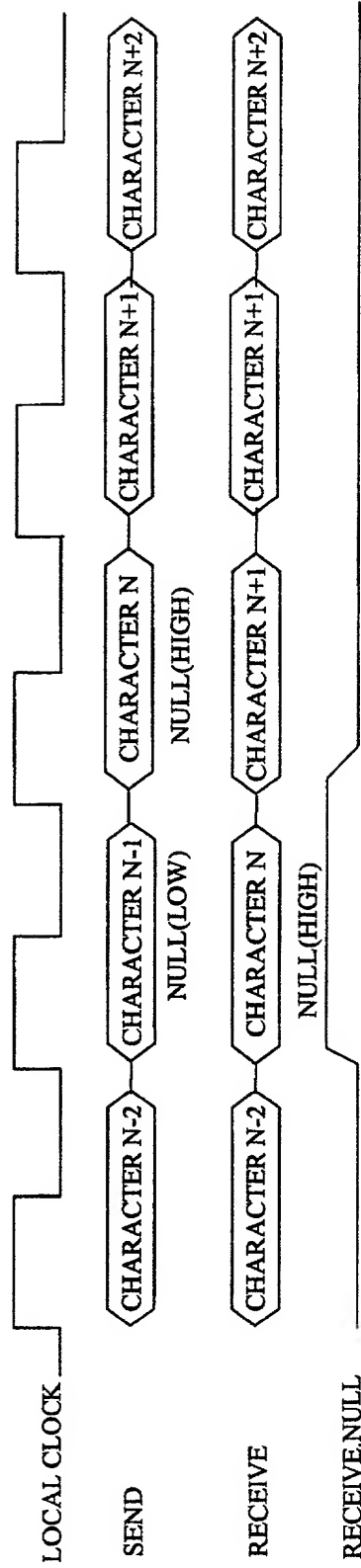


Fig 49B